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FH MONDAY

13 March 2023

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EdgeQ to Debut Single Chip for 5G Private Networks

EdgeQ, a startup led by former Qualcomm executives, plans to introduce its first chip for 5G private networks in the middle of this year. Before that, the company is set to hold a technology demonstration with customer Vodafone at the Mobile World Conference (MWC) in Barcelona near the end of February.

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TALK TO US

STMicroelectronics Expands Portfolio of RF IPDs

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Arteris, SiFive team for RISC-V edge AI reference

On-chip networking specialist Arteris has signed a partnership deal with RISC-V core developer SiFive to help speed up the development of industrial and consumer chips for edge AI.

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Startup AiM Future Set to Commercialize LG's AI IP

AiM Future, a spinout from LG Electronics, is commercializing the Korean consumer giant's AI acceleration IP for applications as diverse as consumer electronics, robotics and automotive. The IP is designed for multi-modal operation, running many different AI models at once. The current hardware generation also supports training at the edge, and future generations aim to extend efficient scaling above the current tens of TOPS range.

LG spun out its semiconductor and IP divisions in 2020, prior to exiting the mobile phone market in 2021. AiM's founders were LG employees working on the company's AI accelerator IP in its Silicon Valley lab at the time; they were able to raise a seed round of $1.8 million and will be closing a $6.1 million-Series A shortly. LG is a lead investor, and will be a potential customer for AiM when it commercializes the IP it's developed since spinning out later this year, AiM Future CEO ChangSoo Kim told EE Times.

EdgeQ to Debut Single Chip for 5G Private Networks

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EdgeQ CEO Vinay Ravuri sat down for an interview with EE Times about the company's plans to kickstart the 5G private network business. Some say the "Q" in EdgeQ stands for Qualcomm.

"Some people do joke, 'It's Qualcomm with an edge,' and it's Qualcomm this and that," Ravuri said. "But no, it's not meant to be any of those. The genesis of the company is to merge compute and connectivity together."

SEMCO Develops Semiconductor Substrate for Autonomous Driving

Samsung Electro-Mechanics announced on Feb. 26 that it has developed an automotive semiconductor substrate applicable to advanced driver assistance systems (ADAS), and will expand its lineup of high-end automotive semiconductor substrates.

The newly developed flip chip ball grid array (FCBGA) is a substrate for high-performance autonomous driving (ADAS) systems and is one of the most technically challenging products among automotive products.

Samsung Electro-Mechanics plans to supply this product to global customers and target the electric vehicle market with the aim to become the global No. 1 company in high-end automotive semiconductor substrates.

STMicroelectronics Expands Portfolio of RF IPDs for STM32WL MCUs

STMicroelectronics has expanded its portfolio of RF integrated passive devices (RF IPDs) by releasing nine new devices that combine antenna impedance-matching, balun, and harmonic-filter circuity optimized for STM32WL wireless microcontrollers (MCUs).

ST's STM32WL MCUs combine application-level processing and wireless communication for smart, connected devices, by integrating an Arm Cortex-M4 MCU with a sub-GHz long-range radio managed by a Cortex-M0+ core. The radio is LPWAN compliant, supports multiple modulation schemes, and comes with LoRaWAN and Sigfox stacks included in the STM32CubeWL MCU software package.

Arteris, SiFive team for RISC-V edge AI reference design

On-chip networking specialist Arteris has signed a partnership deal with RISC-V core developer SiFive to help speed up the development of industrial and consumer chips for edge AI.

Combining the SiFive Intelligence processor IP and Arteris Ncore interconnect IP accelerates the development of chips that can run machine learning frameworks, simplifying the complex verification and validation stage of the design by running the IP on an FPGA.

SiFive Intelligence X280 multi-core capable RISC-V processor IP enables various data-driven applications, including AI inference, image processing, data centre acceleration and other use cases. Arteris Ncore cache coherent interconnect IP is a configurable and scalable network-on-chip (NoC) interconnect for heterogeneous cache coherent systems-on-chip (SoCs).