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Research Brief: 2019/01 – The Planar IC Process

The Planar IC Process

On 1 December 1957, Jean Hoerni, a Swiss physicist and Fairchild Semiconductor co-founder, recorded in his patent notebook an entry called "A method of protecting exposed p-n junctions at the surface of silicon transistors by oxide masking techniques." This was the first formal documentation of the planar semiconductor process, a radically new transistor design in which the oxide layer was left in place on the silicon wafer to protect the sensitive p-n junctions underneath.

Focused on getting its first semiconductor devices into production, Fairchild did not pursue Hoerni's planar approach at that time and it was not until 14 January 1959 that Hoerni finally wrote up his disclosure for what would become U.S. Patent 3025589. One week later, on 23 January 1959, Robert (Bob) Noyce, a fellow Fairchild co-founder, wrote up a disclosure for the planar IC.

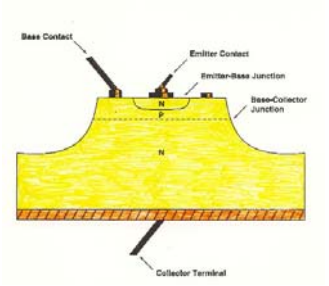
Fairchild's first working planar IC was built some 16 months later in May 1960. Sixty years on, this technology remains the basis for virtually all semiconductor manufacturing today.

The Early Days

By the late 1950s, even though barely a decade old, transistors had already gone through several stages of development, including the material transition from germanium to silicon and the move from piece by piece to batch manufacturing through a simple photolithographic and

etching technique known as the Mesa process. This name reflected the transistor's cross-sectional similarity to the windswept corners of the Grand Canyon in Arizona with its isolated, flat-topped elevations, ridges or hills (mesas), bounded on all sides by steep escarpments standing above the surrounding plains.

Figure 1: - Mesa Transistor Structure vs. Geographic Hills



Source: Computer History Museum

Source: National Geographic

Given that the transistor base was composed of negatively doped silicon and the collector and emitter positively doped, the world's first planar devices were pnp transistors.

Whilst the mesa process clearly had significant manufacturing benefits, it suffered from two major drawbacks, namely its proud surface structures were susceptible to both physical and contamination damage, and subsequent reliability problems, and the process was not suitable for making resistors.

Whereas reliability issues were a significant industry problem at the time, especially for space applications which was one of the then main transistor markets, the non-suitability to make resistors was yet to rear its head, eventually rendering the mesa process completely unsuitable for ICs.

Seeking a solution to the mesa transistor reliability issues, Hoerni revisited his December 1957 idea. Instead of mounting the transistor base on top of the silicon (the 'mesa'), he diffused it into the silicon substrate and then diffused the emitter into the base. In this way he created a flat (planar) structure, covering the whole surface with a protective coating of insulating silicon dioxide leaving just areas in the base and the emitter uncovered.

This all-important breakthrough resulted in not only a more robust and reliable transistor, but also paved the way for the production of commercial ICs.

IC Development

In July 1958, Jack Kilby of Texas Instruments, conceived the world's first IC. He went on to construct the first working prototype using germanium mesa p-n-p slices etched to form transistor, capacitor and resistor elements. On 12 September 1958, using fine gold wires, Kilby

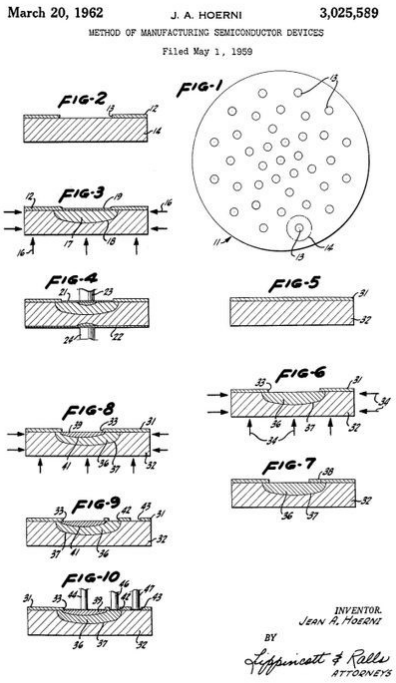
successfully connected the separate elements into an oscillator circuit and, a week after that, demonstrated an amplifier as well.

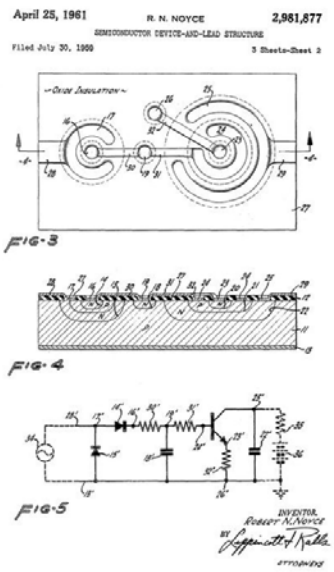
On 6 February 1959, Kilby filed an application, ‘Miniaturized electronic circuits’, for U.S. Patent 3138743.

As mentioned earlier, Noyce’s first patent notebook disclosure of his invention "Methods of isolating multiple devices" was on 23 January 1959. This entry suggested diffusing a thin layer of aluminium into the elements in order to create the connections to the outside world and was the basis of Noyce’s U. S. Patent 2981877 application filed on 30 July 1959.

The stage was thus set; let the mesa vs. planar battle begin. On the one hand, Kilby had the earliest IC patent, but his devices were hybrid, comprising of several etched mesa active and passive elements, connected together by ‘flying wires’. In contrast, the Fairchild IC solution was monolithic, combining Hoerni’s planar process with Noyce’s interconnection via a diffused layer of metal conductors.

Figure 2: - Hoerni & Noyce Fairchild Patent Notebook Entries


March 20, 1962 J. A. HOERNI 3,025,589
METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES
Filed May 1, 1959
FIG-1
FIG-2
FIG-3
FIG-4
FIG-5
FIG-6
FIG-7
FIG-8
FIG-9
FIG-10
INVENTOR.
JEAN A. HOERNI
BY
Lippincott & Ralls
ATTORNEYS


April 25, 1961 R. N. NOYCE 2,981,877
SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE
Filed July 30, 1959
FIG-3
FIG-4
FIG-5
INVENTOR.
ROBERT N. NOYCE
BY
Lippincott & Ralls
ATTORNEYS

Jean Hoerni’s planar process patent “Method of manufacturing semiconductor devices” (U.S. Patent # 3.025,589) filed in May 1959

Robert Noyce’s planar IC patent, "Semiconductor device-and-lead structure" (U. S. Patent # 2981877) filed in July 1959

Source: Fairchild Semiconductor / Computer History Museum

Figure 3: - Early Prototype ICs

Early Texas Instruments 'Flying Wire' IC, function unknown – March 1960

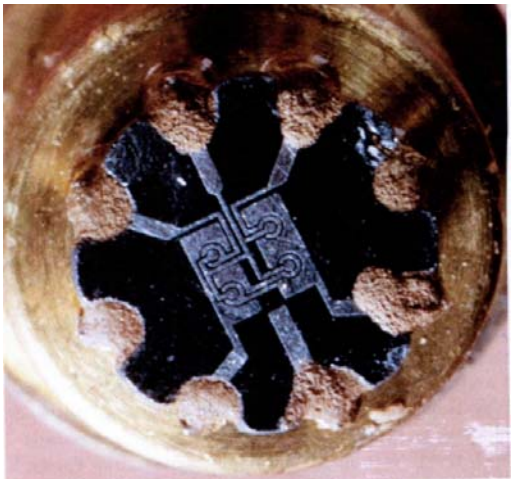
First Prototype Planar IC integrating four transistors and six resistors – May 1960

Source: Fairchild Semiconductor / Computer History Museum

Following the 30 July 1959 patent application, in August 1959, Noyce asked Fairchild co-founder and Head of IC Development, Jay Last, to begin development of an IC based on the planar process. Last's team, which included Sam Fok, Isy Haas, Lionel Kattner and James Nall, having analysed characterization data from Don Farina and Robert Norman From Fairchild's Applications' Department, used modified Direct Coupled Transistor Logic (DCTL) to design a flip-flop with four-transistors and five resistors.

The first planar working devices were produced on 26 May 1960 but used physical isolation to electrically separate the various components. This was subsequently replaced by an innovative boron diffused isolation technique, pioneered by Haas and Kattner, with fully debugged working devices on 27 September 1960.

Figure 4: - World's First Planar IC – May 1960



Source: Fairchild Semiconductor

Figure 5: - Original Planar Process Flow

1. N-Si substrate polishing (80 µm ± 5 µm)
2. Oxidation (wet oxide 8000 Å)
3. MASK 1 (Isolation)
4. Wet etch oxide
5. Boron Deposition and Drive-in
6. MASK 2 (Base and P-Resistor)
7. Boron diffusion (~ 6000 Å oxide, ~ 150 Ω/sq
8. MASK 3 (Emitter and Collector Contacts)
9. Phosphorus Deposition and Drive-in (~ 2 Ω/sq and X_j ~ 1.4–1.6 µm)
10. Resist (front side)
11. Wet etch oxide (back side only)
12. Vacuum Evaporation of Gold on the back side (~ 400 Å)
13. Gold Diffusion (~ 1050°C/~ 15 min with fast cool)
14. MASK 4 (Contacts)
15. Evaporate Aluminum (front side, 0.01 Ω/sq)
16. MASK 5 (Metal)
17. Wet etch metal (25% solution of sodium hydroxide)
18. Metal alloying (~ 600°C/ Argon)

Source: Fairchild Semiconductor

Encouraged by this success, Fairchild started delivering prototype samples to their customers for evaluation and made technical presentations at various engineering conferences.

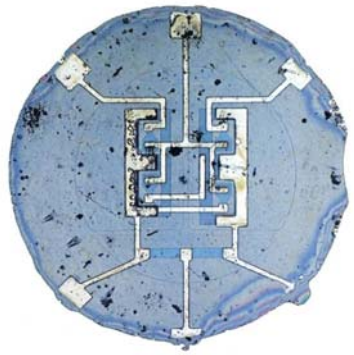
The ICs were official launched under the µLogic (Micrologic) trade name at the IRE Convention in the Waldorf-Astoria Hotel, New York on 21 March 1961.

Figure 6: - Micrologic Advert – Electronic News, 8 May 1961

Source: Fairchild Semiconductor

The first production circuit was the type "F" flip-flop, with six additional circuits, including the type "G" gate, a half adder, and a half shift register, introduced in October 1961. The circuits were all designed by Bob Norman and Bob Anderson.

Figure 7: - Fairchild Micrologic “F” Type Flip-Flop



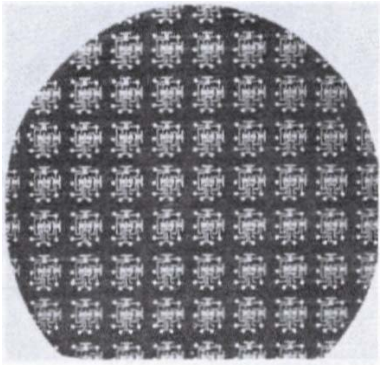
Source: Fairchild Semiconductor

Figure 8: - Fairchild Micrologic (μLogic) Family

1.	“F” Type	Flip-Flop (4 transistors, 2 resistors)
2.	“S” Type	Half-Shift Register (9 transistors, 5 resistors)
3.	“G” Type	Gate (3 transistors, 1 resistors)
4.	“B” Type	Buffer (3 transistors, 3 resistors)
5.	“H” Type	Half-Adder (4 transistors, 3 resistors)
6.	“C” Type	Counter Adaptor (6 transistors, 5 resistors)
7.	“R” Type	Shift Register (17 transistors, 9 resistors)

Source: Fairchild Semiconductor

Figure 9: - “S” Type Half-Shift Register Die On 1” Wafer



Source: Fairchild Semiconductor

"F" Type yields were typically only 5 percent, primarily due to poor mask alignment. That would equate to around US$ 30 per square inch in revenue, a value that has proved remarkable constant throughout the sixty-year IC industry history!

Planar? No Brainer

Texas Instruments introduced the world's first commercial IC, the Type 502 Binary Flip-Flop, in March 1960. It was essentially a hybrid IC, using 'flying-wire' interconnections, and priced at $450 each. Not only was this prohibitively expensive, the technique did not readily lend itself to high-volume manufacture.

In contrast, the Fairchild "F" Type equivalent fully integrated monolithic planar device was both readily manufacturable and significantly cheaper at just $120.

With the writing on the wall, Texas Instruments quickly adopted Jean Hoerni's planar technique and, in October 1961, announced its competitive Series 51 DCTL "fully-integrated circuit" family.

The rest, as they say, is history.

23 Jan 2019