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Future Horizons Ltd, • 44 Bethel Road • Sevenoaks • Kent TN13 3UE • England Tel: +44 1732 740440 • Fax: +44 1732 740442 e-mail: <u>mail@futurehorizons.com</u>• <u>http://www.futurehorizons.com/</u> Affiliates in Europe, India, Israel, Japan, Russian, San Jose California, USA

5G O-RAN mMIMO Radio for Next-Gen Communication

Analog Devices Inc. (ADI) and NEC are collaborating to provide 5G O-RAN massive MIMO (mMIMO) radio for Rakuten Mobile. ADI's fourth-generation software-defined radio is designed to support wireless applications such as massive MIMO and small cell systems, simplifying design and lowering power consumption. The radio unit has a 5G open vRAN (virtual RAN) interface corresponding to Rakuten Mobile's virtualized end-to-end native cloud mobile network. The system performs digital pre-distortion in addition to digital beamforming.

In an interview with EE Times, Joe Barry, VP of Wireless at ADI, said, "Rollouts are progressing from coverage to capacity deployments with standalone 5G functionality, and we're seeing the potential of virtualization of the networks. This effort is establishing the first leg of 5G — ultra-high-speed mobile data access to the mobile user. Achieving the full potential of 5G will come from reaching the emerging opportunities in Industrial, Transportation, Medical and immersive consumer markets. With such a diverse set of use cases across so many markets, robust and disruptive ecosystems are required to tackle these challenges."

Cambridge Wireless, Huawei Plan 5G Network in Science Park

Cambridge Wireless (CW) has teamed up with Huawei to build a 5G mobile private network on the Cambridge Science Park, as part of a testbed due to go live in January 2021.

The new set-up will allow companies on the Cambridge Science Park to explore how advanced wireless technology can have a far-reaching impact on both society and the economy. With over 120 companies on the park, they will be encouraged to undertake research and trial applications using 5G in key areas such as autonomous vehicles, clean energy and remote surgery.

It is part of three-year partnership between CW and Huawei, which will involve digital training, business support and joint events. CW said that it had contracted with Freshwave, a network service provider to build the network. Abhi Naha, chief commercial officer at CW, told EE Times Europe that the network will be a light proof-of-concept network which will provide a testbed to see how they can get companies to use 5G to solve specific challenges. He added, "We are looking for organizations who would like to create, accelerate and test out new and innovative applications and products on the CW 5G testbed."

Apple M1 Processor, Passing on the Chiplets

Recent angry comments to EE Times' interview with Intel's Ramune Nagisetty disparaged the current heterogenous integration and chiplet discussions as more of a rehash than an innovation and furthermore simply a way for American manufacturers to obfuscate their inability to stay at the leading edge of wafer fabrication. Although a great deal of the package-level integration that has been discussed is not ground-breaking innovation, there is little doubt that we are in the middle of a significant shift in integration away from system-on-chip (SoC) design.

Espousing the virtues of the SoC approach after that introduction is odd timing, but the latest foray into chip design at Apple was just announced. The M1, based around a custom piece of Apple SoC silicon, will power the new Macbook Air as well as some Macbook Pro and Mac Mini models. If we can take the promotional images provided by Apple at face value, calling the M1 processor die an SoC is certainly no understatement.

FeFET Memory Startup Gets \$20m to Turn Logic Into Memory Cells

The Ferroelectric Memory Company (FMC), a startup in Dresden, Germany, has raised \$20 million in an oversubscribed series B funding round, to bring its ferroelectric field-effect transistor (FeFET) memory solution to the non-volatile memory market.

In an interview with EE Times, Ali Pourkeramati, CEO of FMC, said there's considerable interest in its FeFET memory. The company has exclusive license to two fundamental FeFET patents through the Technische Universität Dresden (TUD). The company was spun out from TU Dresden in 2016 by its co-founders Stefan Muller and Menno Mennenga.

Arm MicroNPU Comes To Application Processors

Arm has created a new version of its microNPU (neural processing unit) IP that is suitable for use alongside Cortex-A CPU cores in application processors. Lead licensee NXP plans to use this IP in an upcoming family of application processors that can handle AI application such as pose estimation, multi-face recognition and object detection in videos, and speech recognition beyond basic keyword spotting.

Arm's existing microNPU product, the Ethos-U55, launched in February 2020, is aimed at microcontroller-class products alongside Cortex-M cores. It provides up to 0.5 TOPS of acceleration (based on smaller geometries such as 16 or 7 nm, running at 1 GHz), with between 3 and 256 multiply-accumulate units (MACs). Arm's portfolio also has the Ethos-N77, N57 and N37 which offer 4, 2 and 1 TOPS, respectively.