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SEMI and EDA Industry Leaders Unite to Combat Software Piracy

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TALK TO US

Marvell Targets Enterprise Edge with new Switch and PHY Portfolio

Growing remote workforces and future 5G and Wi-Fi 6 deployments mean that enterprises will become increasingly borderless. This entails a move from data center to the enterprise edge, and Marvell intends to capitalize on the trend with the introduction of a portfolio of Ethernet switches and PHYs that integrate security, analytics and visibility to enable an intelligent edge.

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Ultra-low-jitter clock oscillators optimized for optical DSPs

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SEMI and EDA Industry Leaders Unite to Combat Software Piracy

MILPITAS, CALIF. — August 4, 2020 — SEMI, Cadence, Mentor, a Siemens Business, and Synopsys today announced plans to jointly develop an industry-standard protocol to combat electronic design automation (EDA) software piracy, a growing and costly problem for software vendors and their users. Under the partnership, the organizations will develop the SEMI Server Certification Protocol, a standard that will provide strong protection against piracy by defining how servers can be uniquely identified.

Currently, most software license management systems rely on a license manager that runs on a server typically identified by a machine identifier. The problem is that software pirates can clone the machine identifier due to virtualization technologies, to gain illegitimate access to many additional licenses without added cost.

“This joint development effort highlights SEMI’s ability to gather industry players to solve critical problems,” said Bob Smith, the ESD Alliance’s executive director. “We look forward to working with EDA industry leaders Cadence, Mentor and Synopsys to develop this much-needed protocol that will provide protection against piracy.”

New NVM Architecture Could Open Up Xpoint Market

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Intermolecular Inc., a wholly-owned subsidiary of Merck KGaA, Darmstadt, Germany, recently announced it has developed what it believes is the first quaternary atomic layer deposition (ALD) GeAsSeTe OTS device for 3D vertical memory arrays. This device overcomes the inability to stack tens of layers in a 3D structure, which limits memory density and results in higher costs, said Intermolecular device engineer Mario Laudato. The company’s new material combination can help to realize these architectures, which would support emerging use cases such as artificial intelligence (AI) and neuromorphic computing, and other semiconductor designs necessary for faster and more affordable digital applications.

Startup Claims Low-power IoT Geolocation Without a Positioning Chipset

Smartphone and in-vehicle navigation systems have some drawbacks. Localization accuracy in critical indoor and dense urban environments is often insufficient, and smartphone batteries drain faster. These challenges multiply when faced with the constraints and requirements of IoT applications. Paris-based Nestwave has decided to take a different approach to IoT geolocation and claims improved indoor sensitivity, better accuracy, and shorter time-to-first-fix.

Founded in 2014, Nestwave provides hybrid geolocation IP cores for integration within an IoT modem such as NB-IoT, Cat M1, LoRa, or Sigfox. The patented solution is claimed to improve accuracy in urban canyon environments, to reduce the power consumption and the cost when compared with existing solutions (2.5x accuracy and 1/10 of the power consumption at 1/3 of the cost of GNSS solutions).

Marvell Targets Enterprise Edge with new Switch and PHY Portfolio

Growing remote workforces and future 5G and Wi-Fi 6 deployments mean that enterprises will become increasingly borderless. This entails a move from data center to the enterprise edge, and Marvell intends to capitalize on the trend with the introduction of a portfolio of Ethernet switches and PHYs that integrate security, analytics and visibility to enable an intelligent edge.

According to Sameh Boujelbene, senior research director at telecoms research firm Dell’Oro Group, the growth of 5G, Wi-Fi 6 and internet of things (IoT) devices on the network means that enterprise switching will continue to extend beyond the traditional on-premises campus environment with increasing deployments at the access and intelligent edge. She commented, “These deployment use cases are driving emerging requirements in terms of security, analytics, visibility and automation. Marvell’s new Prestera switch portfolio helps address those requirements.”

Ultra-low-jitter clock oscillators optimized for optical DSPs

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Raltron Electronics Inc. has introduced a new series of ultra-low-jitter clock oscillators, targeting high frequency digital signal processors (DSPs) in optical applications. These new oscillators address the demand for lower jitter clocks to reduce noise in systems as network bandwidths increase with faster data rates.

DSPs used inside optical transceivers at both ends of the fiber optic link enable increased transmission speeds all the way to 800G, simpler circuitry, and improved optical performance, said Raltron, requiring high frequency, ultra-low-jitter clock oscillators, VCXOs, and VCSOs as a frequency reference.