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Intel looks to 1nm for trillion transistor 'chips'

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TALK TO US

Rain Demonstrates AI Training on Analog Chip

Rain Neuromorphics has trained a deep learning network on an analog chip—a crossbar array of memristors—using the company's analog-friendly training algorithms.The process required many orders of magnitude less energy compared with today's GPU systems

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Lattice Expands Into Mid-Range FPGAs

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Embedded AI Solutions Ease ML Development

STMicroelectronics has released upgrades to both NanoEdge AI Studio and STM32Cube.AI to accelerate embedded artificial intelligence (AI) and machine learning (ML) development projects. These tools facilitate moving AI and ML to the edge of an application. At the edge, AI/ML delivers substantial advantages, which include privacy by design, deterministic and real-time response, greater reliability, and lower power consumption.

NanoEdge AI Studio is an automated ML tool for applications that do not require the development of neural networks. It is used with STM32 microcontrollers (MCUs) and MEMS sensors that include ST's unique embedded intelligent sensor processing unit (ISPU). For developers needing to use neural networks, STM32Cube.AI is an AI model optimizer and compiler for STM32. The two new releases deliver features that help design and implement high-performance AI/ML solutions quickly and with minimum investment.

Monolithic GaN optoelectronics on silicon

Researchers in China and Japan have demonstrated a monolithic gallium nitride (GaN) optoelectronic system on silicon (Si) substrate consisting of a transmitter, modulator, waveguide, beam splitter, receivers and monitor [Hao Zhang et al, Appl. Phys. Lett., v121, p181103, 2022].

The team from China's Nanjing University of Posts and Telecommunications and Zhengzhou University and Japan's Nagoya University are seeking to promote optoelectronic systems with low power consumption while using monolithic integration on silicon to reduce material, processing and packaging costs.

The researchers comment: "We propose monolithic, top-down approaches to build III-nitride transmitter, modulator, waveguide, beam splitter, receiver and monitor as a single unit onto a conventional GaN-on-silicon wafer without involving regrowth or postgrowth doping."

Intel looks to 1nm for trillion transistor 'chips

Intel has detailed three areas of research that will put a trillion transistors into a package.

Pat Gelsinger, CEO of Intel, highlighted this strategy back in August, and the company is showing some of the supporting research at the IEEE International Electron Devices Meeting (IEDM) in the US this week.

The research has a number of strands, from chiplet 3D packaging technology that gives a 10x improvement in density as well as 2D materials for 1nm transistors beyond RibbonFET that are just 3 atoms thick and new stackable ferroelectric memories.

Intel needs to compete in the technology roadmap against TSMC and Samsung for the fledgling Intel Foundry Service (IFS) as both have plans to 1nm.

Rain Demonstrates AI Training on Analog Chip

Rain Neuromorphics has trained a deep learning network on an analog chip—a crossbar array of memristors—using the company's analog-friendly training algorithms.

The process required many orders of magnitude less energy compared with today's GPU systems. While Rain's initial work has proven AI can be trained efficiently using analog chips, commercial realizations of the technology may still be a few years away.

In a paper co-authored with memristor pioneer Stanley Williams, Rain describes training single- and two-layer neural networks to recognize words written in braille. The setup uses a combination of two 64 x 64 memristor crossbar arrays (in this case, not the 3D ReRAM-based chip the company previously showed), combined with training algorithms using a technique called activity difference, which includes Rain's earlier work on equilibrium propagation. Rain calls this hardware-algorithm combination memristor activity-difference energy minimization (MADEM).

Lattice Expands Into Mid-Range FPGAs

Lattice Semiconductor, previously known for its small, low-power FPGAs, is entering the mid-range FPGA market in a move that will double the company's addressable market to approximately $6 billion.

Lattice has announced a new technology platform for its mid-range FPGA products, Avant, and the first series of mid-range FPGAs to be built on this platform, the Avant-E series, with up to 500 thousand logic cells.

When we were concepting Avant, we went out and talked to over 100 customers worldwide, in all geographies, in all of our major verticals, to understand what it is they were looking for," Jay Aggarwal, director of silicon product marketing at Lattice, told EE Times. "What we heard from them was resounding—they're looking for innovation in the mid-range space, because the mid-range FPGA space has been overlooked by our competition, who've focused on their high-end devices."