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FH MONDAY

31 October 2016

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Intel, ARM Battle over IoT

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TALK TO US



Cadence Breaks Down Automotive ISO 26262

As automakers start adding more and more Advanced Driver Assistance Systems (ADAS) features, the complexity of software code and SoCs deployed inside vehicles has been skyrocketing.

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Samsung certifies Cadence tools for 10nm process

Samsung Electronics has certified Cadence Design Systems' complete suite of digital and signoff tools for its process design kit (PDK) and foundation library on the company's second-generation 10nm low power plus (LPP) process.

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Fujitsu Eyes Architecture To Rival Quantum Computers

Fujitsu Laboratories Ltd is collaborating with the University of Toronto to develop a computing architecture to tackle combinatorial optimisation problems. The architecture employs conventional semiconductor technology with flexible circuit configurations to allow it to handle a broader range of problems than current quantum computing can manage.

Tough decisions

Certain decisions need to be based on arriving at the most favourable set of parameters from an enormous number of possible combinations. Real-world examples of this include determining procedures for disaster recovery, optimising an investment portfolio and formulating economic policy.

For such combinatorial optimisation problems, as the number of elements involved increases, the number of possible combinations increases exponentially. To solve these problems quickly enough for any practical use, you would need a dramatic increase in computing performance.

Intel, ARM Battle Over IoT

The battle for the Internet of Things heats up this week as Intel and ARM fire off competing announcements to establish their microprocessor architectures on its broad frontiers.

Intel announced its first Atom SoC with real-time capabilities tailored for automotive and industrial markets. Less than two miles away from Intel's headquarters, ARM kicked off its annual developer's conference with news it is bringing hardware security to its lowest-end microcontroller cores.

ARM has a clear lead in the emerging ground game for end nodes with its Cortex-M microcontrollers. Intel, the world's largest semiconductor company, ranks 17th among MCU vendors with its relatively new Quark x86 chips, making it about equal with Panasonic and Sharp according to market watcher IHS Inc.

Samsung's Battery Problem Highlights Broader Engineering Issues

Given the relative rarity of the battery problems with Samsung's smartphone, how do you determine the root cause with confidence?

We're all aware of the serious battery problems which occurred with the recently introduced Samsung Galaxy Note 7 smartphone, leading to its recall followed by complete product withdrawal from the market. While there has been some of the usual sniping at engineers by people who have no idea what product design and release actually involve, I'm pleased to see that it has been relatively muted. Perhaps the critics and comedians have been distracted by the US election, which certainly has provided more "theater" and possibilities for humor and smarmy sarcasm than a smartphone?

Cadence Breaks Down Automotive ISO 26262

As automakers start adding more and more Advanced Driver Assistance Systems (ADAS) features, the complexity of software code and SoCs deployed inside vehicles has been skyrocketing.

This trend puts automotive tech suppliers — chip companies and software vendors — under tremendous pressure to prove the functional safety of their products. They must test and verify safe operation of their electronic devices and codes.

The ISO 26262 functional safety standard not only provides detailed processes for component suppliers to follow, but also asks for documented proof that they followed the standard and that the software tools they used for development are also compliant.

Samsung Certifies Cadence Tools For 10nm Process

Samsung Electronics has certified Cadence Design Systems' complete suite of digital and signoff tools for its process design kit (PDK) and foundation library on the company's second-generation 10nm low power plus (LPP) process.

Samsung, which has recently certified a design platform from Synopsys, has also validated the Cadence reference flow using a quad-core design with the ARM Cortex-A53 processor on the 10LPP process, which was implemented with the low-power design methodology covering power-gating and memory retention, IEEE 1801 UPF2.1 power intent, and statistical on-chip variation (SOCV)-based timing closure using the Liberty Variation Format (LVF) library.

The Cadence signoff tools that have been certified for tape-out using Samsung's certification criteria for baseline accuracy include the Innovus Implementation System, which enables larger designs and reduced turnaround time while supporting Samsung's 10LPP design requirements, such as floorplanning, placement and routing with integrated colour-/pin-access /variability-aware timing closure and clock tree and power optimisation.