DECISION
17 rue de l'Amiral Hamelin
75116 PARIS – France
phone: + 33 1 45 05 70 13 fax: + 33 1 45 05 72 65

www.decision.eu

FUTURE HORIZONS
44 Bethel Road
Sevenoaks, Kent
TN13 3UE – England
phone: +44 (0)1732 740440 fax: +44 (0)1732 740442

www.futurehorizons.com

SMART 2010/062:

Benefits and Measures to Set Up 450mm Semiconductor Prototyping and to Keep Semiconductor Manufacturing in Europe

- The role of Public Authorities and Programmes -

Final Report

The opinions expressed here are those held by the study team at the time of publication of this Report and do not necessarily represent the Commission's official position.

Date: 16th February 2012

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Table Of Contents

List Of Figures

This study was assigned in December 2010 by the European Commission – DG Information Society and Media (DG INFSO) – Directorate Components & Systems (Dir G) – Unit Nanoelectronics (G1), to DECISION in partnership with Future Horizons.

It has been conducted from January 2011 to February 2012 by the following study team:

DECISION:

- Didier Coulon: General Manager (coordinator of the study)
- Sebastien Rospide: Senior Consultant (project manager)

Future Horizons:

- Malcolm Penn: Chief Executive Officer
- Mike Bryant: Chief Technical Officer

supported by two independent industrial experts:

- Laurent Bosson
- Guy Dubois

For further information, please contact:

Willy van Puymbroeck

Head of Unit G1 – Nanoelectronics (DG INFSO)

willy.vanpuymbroeck@ec.europa.eu

+32 (0)2 296 81 38

1. Executive Summary

European semiconductor industry at a crossroads

Europe will lose advanced and competitive semiconductor (hereafter SC) manufacturing infrastructure without a European long-term industrial vision guiding and enabling the coordination of all stakeholders.

Semiconductors is a strategically important industry, providing the knowledge and technologies that generate some 10 percent of global GDP. Its high leverage on innovation cycles and wealth creation makes it one of, if not 'the' most important Key Enabling Technologies for Europe and an essential pillar of any European industrial policy.

Wafer scale-ups always bring disruptions and dislocations in the SC industry. Among the most noteworthy are increased industrial consolidation and concentration and the setting of new competitive standards and rules defined by those driving the wafer transition.

The next scale-up from 300mm to 450mm wafer diameter processing is now a certainty and 450mm fabs will be in full production before the end of the decade.

It will very likely be the final wafer scale up for the industry and will define the geographical locations of the next (and perhaps final) ten to fifteen most advanced semiconductor production areas worldwide.

Europe was at the leading edge during the 200mm to 300mm transition with the 1999 Siemens-Motorola joint venture R&D fab in Dresden the location of the first 300mm fab in the world but failed to capitalize on this strength due to continuous lack of investment especially over the last decade. It is now at a crossroads, with only three 300mm fabs and a steady decline in indigenous manufacturing activities.

From a semiconductor supplier perspective, the 450mm transition is promoted by market leaders focused on advanced node manufacturing (More Moore – MM). There is currently no commitment from European IDMs to 450mm with only one firm (STMicroelectronics) even incorporating 450mm into its long-term strategic plan. Indigenous suppliers have indeed leaderships in advanced products based on more mature technologies (More than Moore – MtM) that will continue to be manufactured on primarily 150mm and 200mm for some time to come.

But the fact remains that the transition to 450 mm will impact all levels of the European SC supply chain, from SC fabs suppliers (facilities, equipment & material suppliers) to chip manufacturers and designers, albeit with different timescales and to different degrees, depending on companies activities and portfolios. But nonetheless, all will be impacted.

Not having a 450mm production infrastructure in Europe will thus mean abdicating production of advanced SC technologies, which will sooner or later (10 years) threaten the competitiveness of the current European SC manufacturing base, including technology development and device design.

Note: investing in additional 300 mm fabs in Europe – when spare 300 mm capacity will be available in Asia – following the 450mm production ramp-up will not make economic sense for Europe.

Towards an integrated European 450mm strategy

The transition to 450mm will be more cost efficient than past transitions due to the increased industrial collaboration organised in Albany, NY within the Global 450 Consortium (G450C). Although the collaboration is currently US-led, Europe should play a role in this early development phase as it did in the past. It has key strengths and capabilities to put forward in equipment & material supply, as well as R&D and technology development activities.

Whatever the degree of coordination, the size of investment will nonetheless remain very significant, with total cost of industry transition estimated between US$25 billion and US$40 billion from 2012 up to the time when the early adopters will open their first 450mm volume fab (as early as 2018). 450mm equipment and material development and qualification will concentrate the largest investment between US$15 billion and US$20 billion. The cost of the 450mm transition will come in addition to existing investment in 300mm technology development and thus translate into a significant increase in funding requirement.

In this context, national 450mm strategies do not make sense and a European 450mm 'master plan' is the only sensible scale. It should be based on both a strong industrial commitment and a coordinated position of public authorities (PAs) that are the necessary conditions to leverage the required funding, avoid duplication and concentrate the funding where needed.

A European 450mm master plan should also coordinate with existing initiatives (G450C) and be open to international participation. The acknowledged European leadership in SC R&D activities should be leveraged to reach a critical mass and gain international dimension. Coordination among European R&D institutes on 450mm is critical.

The different exposure to the 450mm transition across the European supply chain calls for a phased approach corresponding to individual players' needs and agendas. Three scenarios are explored in this Report, together with their cost and associated impact for Europe:

- Scenario 1 corresponds to the 'Business as Usual' scenario whereby 450mm R&D would be supported through current cooperative programmes and budget that are currently almost exclusively focused on 300mm. Such a scenario would lead to a continuous decline in SC production activities in Europe and a progressive shift of the equipment & material industry outside Europe.

- Scenario 2 corresponds to a dedicated European master plan to support equipment and material suppliers in the transition to 450mm platforms. To maximize impact and benefits for the industry, a shared programme coordinating the leading European R&D institutes activities could be envisaged to secure the equipment & material industry in Europe, consolidate and even create new leaderships (450E pilot line).

- Scenario 3 finally corresponds to a process of setting up 450mm volume production in Europe with different, non-exclusive, approaches depending on fab ownerships and

technology targets. This includes the concept of a 450mm joint-fab model in Europe between IDMs (Eurofab450) in true partnership with equipment & material suppliers, initially targeting MtM products but providing a European bridge to MM technologies in due time.

Conclusions

Europe will lose advanced and competitive SC manufacturing infrastructure without a European long-term industrial vision guiding and enabling the coordination of all stakeholders. Such a long-term vision shall not oppose 300mm or 450mm but rather consider both in parallel as part of an advanced manufacturing continuum, taking into account all the stages of the SC supply chain.

Europe failed to capitalize on its strength during the 300mm transition, but 450mm could turn into a genuine opportunity to regain the position it once held in SC manufacturing by securing a complete SC supply chain and making sure that the most advanced SC technologies continue to be manufactured on European soil.

It could start in the short term with a five-year programme to urgently set up the 450E pilot line in Europe to support the transition of the European equipment & material suppliers to 450mm and coordinate with the US-led G450C initiative in Albany.

From a chip production perspective, the opportunity of a joint 450mm MtM fab (Eurofab450) between Integrated Device Manufacturers and a private 450mm MM fab should be investigated and progressed in parallel to their natural conclusion. Whatever the outcome, every effort must be expended by the European Commission and national PAs to ensure that all potential locations and especially the current most advanced manufacturing centres in Europe remain favourable places for chip companies to operate in.

High tech industries can only close competitive gaps during technological shifts. The 450mm shift is one of them and most likely the last one for the semiconductor industry: the European semiconductor industry is at a crossroads. The 450mm transition is a unique opportunity to launch a European industrial policy, building on its strengths (R&D, equipment & material, cooperative development) and an increased level of coordination to preserve the remaining manufacturing base in Europe and protect its innovation power in the future.

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2. Overview

For several years now, 450mm wafer processing has been under discussion but apart from work on setting the standards and some prototype equipment, little had actually emerged. Indeed much discussion focused on whether the industry could actually afford to make this transition, how much it would cost and who would pay for it. The European Commission thus decided to undertake this project to determine the future, if any, of 450mm processing and the effect this would have on Europe.

As such, in December 2010, the European Commission awarded a contract to DECISION in partnership with Future Horizons to undertake a study on the activities required to support research and innovation in the field of advanced semiconductor production and measures necessary to attract investments and to support advanced research infrastructures, prototyping and early nanoelectronics manufacturing in Europe with particular emphasis on 450mm manufacturing, including:

- An assessment of the role of the European Commission and Governments of Member States and Regions for the establishment of 450mm manufacturing capabilities, including related value chain aspects, and overall their role in keeping semiconductor manufacturing and advanced nanoelectronics technologies in Europe

- An analysis of potential links between newly established 450mm manufacturing with existing semiconductor manufacturing capabilities and their likely impact on them both at the prototyping and high-volume level

Within weeks of the contract being signed, however, the issue of 'if' it would happen was settled, thanks to a strong joint-announcement made by Intel and TSMC, supported by Samsung. This changed some of the goals of the project making it an even more valid undertaking.

Key parts of the Report include:

- Identification of possible business cases that may assist Europe as a manufacturing base for advanced semiconductors and the effect this may have on existing semiconductor manufacturing in Europe

- An assessment of Europe's current position in semiconductor R&D together with a view on its future prospects

- Details on Europe's position in areas such as semiconductor technology and processes, equipment and equipment technologies, materials and semiconductor manufacturing itself

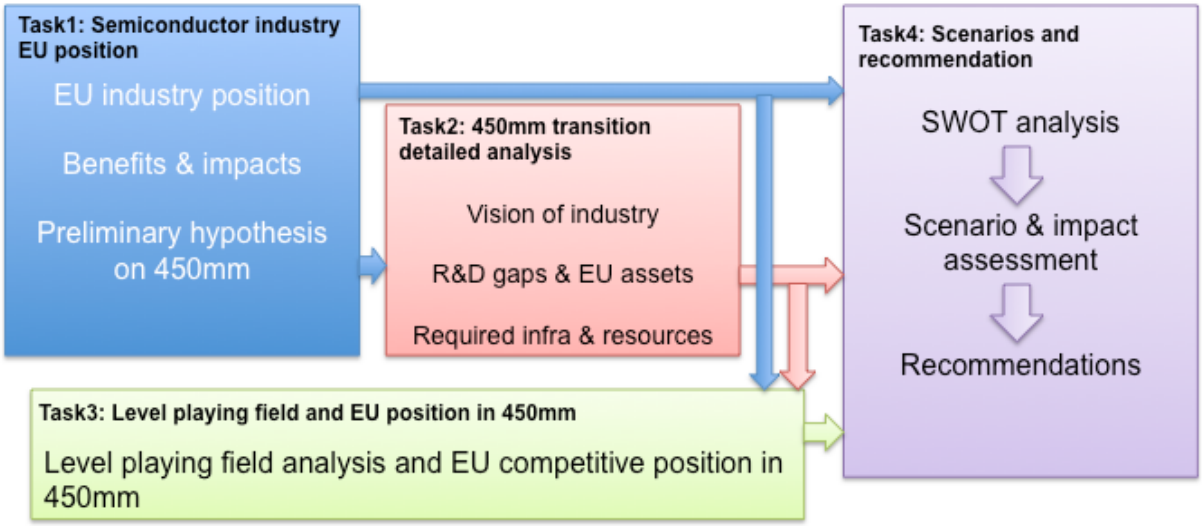
- The degree of public support offered worldwide, both financial and otherwise

- Other 'roadblock' issues which Europe may need to address

The methodology for the study was divided into four specific tasks as shown in Figure 1. Task 1 focused on the business cases for the various possibilities of what Europe's response

to the Intel and TSMC announcements could be. It provided a framework for Task 2, during which a wide range of senior industry executives were interviewed using questions generated by Task 1. Task 3 analysed the 450mm market and funding in much greater detail, whilst Task 4 brings all the results together for the final Report.

Figure 1 – Project Task Flow



Source: DECISION/Future Horizons

The questions used during the consultation process are provided in Appendix 2. The intention of this list was to ensure that interviews covered all the important topics whilst still allowing those being interviewed to add any information they deemed important to the study.

In addition to Task 2 consultations, close links with the industry have been maintained during the study development and a Focus Group was created with the following companies involved:

- Aixtron
- ASML
- ASMI
- BOSCH
- Fraunhofer
- GlobalFoundries
- IDC
- IMEC
- Infineon
- Intel
- Leti
- Lfoundry
- M&W
- NXP
- RECIF
- Samsung
- Siltronic
- Soitec
- STMicroelectronics
- TI
- TSMC

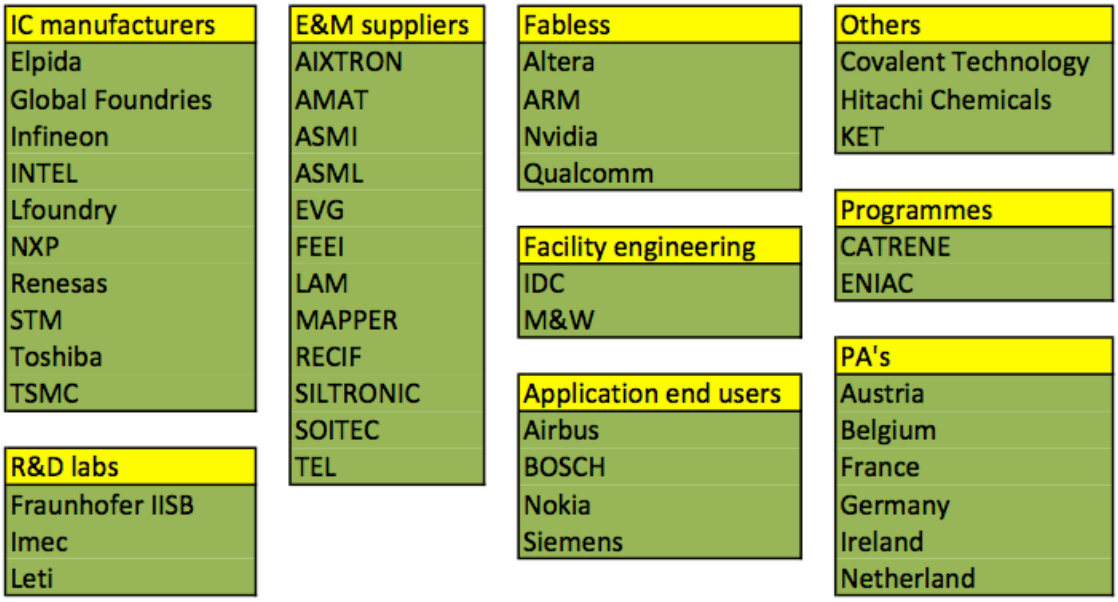
Two meetings of the study's Focus Group were organized in Paris in March and September 2011 to assist the study team at two critical stages of this assignment (validation of stakeholders' interview guide + validation of key findings and scenarios).

Finally, a Steering Group composed of key representatives from EEMI450, INTEL, SEMI Europe and STMicroelectronics was also created with four meetings held with the study team to validate the interim results and provide guidance for the remaining steps.

The information presented in this Report has been derived from Future Horizons' and DECISION's interviews with members of the semiconductor industry worldwide and with the representatives of PAs throughout Europe, together with their combined extensive database and experience in the semiconductor and related industries. The opinions expressed in this Report are those currently held by the authors and may not represent the European Commission's official position. They are subject to future change.

Figure 2 provides the list of companies and organizations directly interviewed within the scope of this assignment.

Figure 2 – Project Interviews



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3. Introduction

At the time of commissioning this Report, the future development of 450mm wafer processing was unclear. Although the standards for the wafer itself and its handling were being prepared, there was a continuing argument that the expense of developing and rolling out the technology could possibly exceed the benefits to be gained from manufacturing at this larger wafer size. Some equipment makers were even still arguing that they had not fully recovered the development cost for the past wafer scale up, from 200mm to 300mm.

As was the case at 300mm, it was clear from the outset that the expense of developing 450mm would require an element of state support, even if this investment would pay for itself in the long-term. Such transitions are also a huge drain on the infrastructure and there is thus the added risk that the short-term redirection of resources would damage the industry in other ways. For example, it has been argued that support for 450mm would divert attention and resources from the more efficient manufacturing processes being developed at the 300mm node, as well as impacting on the MtM approach many companies were adopting.

Overall it would be fair to say that there was still a lot of industry scepticism, with some organisations even wishing that this particular genie would stay locked in its bottle. By March 2011, however, the climate had changed significantly with this particular wish sidelined by Intel and TSMC's near simultaneous announcements that they intended to roll out 450mm wafer technology in their latest fab plants as soon as it was possible.

Of course these are two of the most dominant semiconductor companies in the world, and the ones who can better afford the costs of the transition, leading to comments from some parties that this was simply an attempt by these firms to cement their dominance of the crucial microprocessor, logic and potentially memory industries when, as expected, Samsung committed as well.

This may well be true but it is by no means a certainty; history has shown that leadership positions in the semiconductor industry can often be transitory whereby just one mistake can consign a company to steady decline. It will take a decade to determine whether this transition will be the correct choice for them but in the meantime the rest of the industry will have to respond in the best way it can.

As with previous wafer size changes, the transition to 450mm wafer processing cannot be done overnight, indeed some of the earlier timescales looked highly optimistic, but the intent is now clear and this new wafer size will be introduced. There is also now an increasing consensus on its timing and roll out strategy.

When the project started, we were aware of similar discussions taking place between government and industry in Japan and the US, and expected that Korea and Taiwan would also be having such discussions.

One hypothesis at the beginning of the project was that Europe simply could not afford to directly respond to this transition given it no longer had indigenous semiconductor IDMs demonstrating leadership positions at the most advanced nodes of the technology ladder and, in any case, these companies had moved some of their wafer manufacturing to the Far East whilst relying on foundries for their advanced IC processes.

It was therefore suggested that 450mm technology would simply hasten the divergence of these companies into more specialist areas, such as MtM, at least in the short to medium-term. Not requiring the latest technology today offered Europe the possibility to effectively sidestep the issue for now and instead use its resources to focus on alternative technologies in an attempt to add value to their existing fabs within Europe and elsewhere.

The converse argument, and second option considered, was that Europe had a very successful R&D, materials and production equipment industry, many of whom, for example IMEC and ASML, had globally dominant positions and extensive key IP portfolios in the most advanced processing technologies whilst others had key specialities. These European players were at the forefront of enabling this transition and for them, not just embracing but taking a leading role in the 450mm transition was an absolute priority, regardless of what Europe's indigenous semiconductor IDMs decided to do.

Also to be considered were the needs of Europe's fabless community that, although smaller in size to their mainly US peers, were also highly dependent on advanced semiconductor technologies and as such were currently forced to go to the large Asian-foundries to satisfy their needs. This raised the possibility that Europe could offer direct support to a foreign-owned semiconductor foundry or IDM to encourage them to set up a 450mm wafer fab in Europe.

A third and final option considered was whether semiconductors were still an area that Europe could succeed in or whether it should focus its support into alternative technology areas. Certainly there were many in other fields who strongly argue this case. It would however have been in contradiction to Europe's current position and policy on the strategic importance of semiconductors and their role as one of only six designated Key Enabling Technologies (KETs). Such a decision would therefore have serious long-term ramifications for Europe's overall competitive global position.

Given the wide divergence of these three current options, each of which have many individual company, government and research organisation supporters, all of the options were investigated and evaluated impartially, based on the merits of the arguments and global industry trends.

Key to the final recommendations of our analysis was what would be best for Europe, even though this was almost bound to contradict the strategic policies and preferences of some individual European governments and organisations. Given the wide divergence of views and opinions initially encountered, we were originally concerned that it would be unlikely everyone would be satisfied and happy with the outcome of this study.

Thankfully, however, as the project progressed and the results openly debated at the various company, Steering and Focus Group discussions, we were able to keep the debate focused on the issues rather than individual company or national preferences.

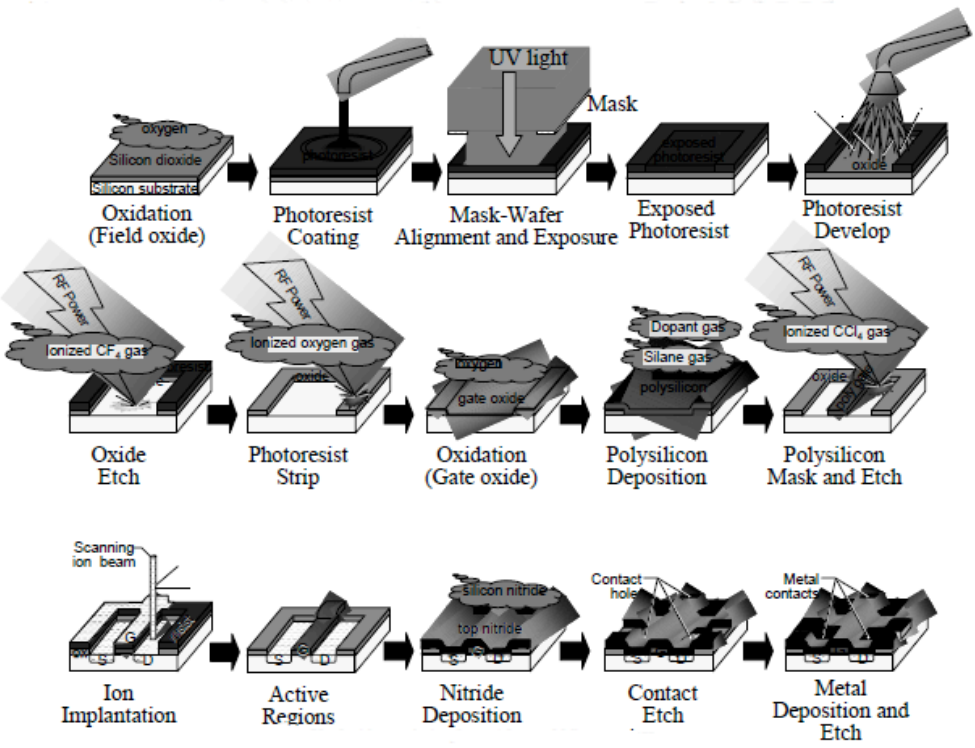
Whilst we do still expect to see individual company, and even national, nuances of interpretation, we are highly confident that this Report represents a fair and honest reflection of today's 450mm transition reality.

4. State-Of-The-Art SC Manufacturing In Europe

4.1. Introduction

Processing a semiconductor wafer of any size is a complex task. The very simplified diagram below shows some of the major processes, though in fact many of these are themselves quite complex and repeated several times. For example, at 28nm there can be up to 12 layers of metal so the final task "Metal deposition and etch" may involve 60-80 process steps alone. In all, the wafer will undergo between 500 to 600 sequential operations from start to finish, each of which must be strictly controlled and managed.

Figure 3 – Simplified Wafer Fabrication Process



Source: AMD

Each process step requires different equipment and each tends to have just one or two suppliers. Probably the key step to the final performance of the IC is the lithography process where a photo-resist coating on the wafer is exposed to an image from a photo-mask. What was once a fairly simple process is now vastly more complex for the simple reason that the wavelengths of the ultraviolet light used to expose the photo-resist are now about an order of magnitude larger than the details on the wafer needing to be etched. Numerous techniques

are used to enhance the accuracy and detail on the resist, the impact of and further details on this will be discussed later.

4.2. IC Manufacturing In Europe

During the 1990s, Europe saw a growth in new fabs but, despite having driven the development of 300mm wafers in an attempt to stop the flow of manufacturing to the Far East, Europe fell significantly behind in semiconductor production during the last decade. Old fabs closed with few new ones opening to replace them. Whereas Europe accounted for approximately 11 percent of world chip production in 2000, its production share has decreased to just under 5 percent in 2011.

With hindsight, the biggest loss during this period was the closing of Qimonda in February 2009 when it filed for bankruptcy, just 1-2 quarters before the memory market staged a dramatic recovery. Their well-equipped 300mm fab was dismantled with some of the equipment auctioned off at well below market value; this now forming the basis of Texas Instruments' transfer of analogue IC production to 300mm wafers in a US fab. This loss however may now be partially recovered following Infineon's decision to purchase the Qimonda cleanrooms and remaining assets 'for 65nm analogue/power IC production', almost certainly as a competitive response to TI's 300mm analogue fab decision.

The other negative event was the failure to facilitate and equip STMicroelectronics' Catania 300mm fab shell which is now been used by 3Sun (a joint venture between Sharp, ENEL and STMicroelectronics) to make PV wafers instead.

The largest fabs currently operating in Europe are those of Intel (Ireland) and GlobalFoundries (Germany), both of which are being significantly upgraded to handle the latest 300mm technologies thereby assuring some high-volume advanced IC manufacture remains in Europe.

At the low-volume end of the scale, STMicroelectronics' plant in Crolles utilises 200mm and 300mm wafers and works down to the 28nm node on the 300mm line. However its capacity is limited to around 17k wafer starts per month versus the 80k per month planned for the GlobalFoundries Dresden complex once the expansion is completed. Crolles is often referred to as a lab-fab where (a) new technologies are developed (b) new products are first run before transfer to foundries and (c) low run-rate, high-value specialist ICs are made, such as STMicroelectronics' huge die area networking ICs.

Finally, at the advanced research level, IMEC has a 300mm clean room that is equipped to the very highest standards and is arguably the best R&D centre in the world. It is already capable of producing 8nm structures, 5nm by hand if necessary, on a par with the world's best, namely IBM, Intel and Toshiba. Leti is primarily focused on advanced SOI processing, resists and mask-less lithography and the combination of Leti's process capability and Crolles 300mm line provides them with a quasi-300mm R&D capability. These advanced research infrastructures are used both for the development of new processes and for testing and working on new equipment from their commercial partners, especially at IMEC.

Extending Europe's 'high-tech borders' to Israel, both the Intel and Micron (ex-Numonyx) fabs there are advanced manufacturing lines but there are now no other meaningful state-of-the-art fabs within Europe capable of processing advanced technology nodes; most others

are 200mm wafer size or less and, as far as we are aware, it seems reasonable to surmise that the existing European manufacturers are not currently considering building new 300mm fabs in Europe.

4.3. European Companies Manufacturing Elsewhere

This dearth of European-based manufacturing plants might be reasonable if European companies had sizeable state-of-the-art fabs located elsewhere, e.g. for reasons of cost. However what plants the European companies do have are far below the state-of-the-art from both a wafer size and technology node perspective. Infineon has a plant in Malaysia making 350nm power devices on 200mm wafers, NXP has nothing and STMicroelectronics produces power devices on 150mm in Singapore, albeit at an impressive over half a million wafers per month level, which does go to show Europe's chip firms do have the expertise to run high-volume wafer fab plants were it mindful to do so.

4.4. The 'Fab-Lite' Alternative

European semiconductor companies have instead all taken the approach of using foundry services from TSMC and others in a strategy labelled 'fab-lite'. Squeezed by a presumption of 'ever-declining' ASPs (no longer true), a more mature single digit market growth in value terms (a questionable extrapolation), and the success of fabless competitors like Broadcom, MediaTek and Qualcomm, many IDMs came to the conclusion that advanced in-house wafer production was both too expensive and unnecessary, with no strategic value or commercial market benefit. This gave birth to the fab-lite business model which was enthusiastically adopted by IDMs everywhere in the last decade to the delight of the financial community as a way of reducing capital requirement whilst still satisfying both the needs of their customers and investors at seemingly zero risk to the supply chain.

Numerous arguments have been provided in support of this move, such as: wafer fabrication has become a service operation, a simple make-buy decision best left to outsourcing; foundries were fundamentally more efficient than IDMs in ramping up production and loading their lines meaning they can make wafers much cheaper than in-house production, especially in advanced technologies; the semiconductor industry has been outsourcing back-end manufacturing for decades without any problem; and fabless companies had constantly out-performed IDM's growth with no competitive disadvantage by not having a fab.

Contrasting this with the IDM having to own and operate a fab, thereby tying up cash and management resources, 'fab-lite' appeared to both solve the inherent fab ownership operational (loading and constant investment need) problems and level the playing field with the IDM's fabless competitors. But the justification and implementation has since become muddled, with terms such as 'asset-lite' or 'asset-smart' introduced, implying these are subtly different and implicitly better than 'fab-lite', casting doubt over the robustness of this business model. Rhetoric aside, there are really only two fundamental 'fab-lite' varieties.

The first option is to maintain a small in-house wafer fab, often known as a 'lab-fab', to prove out each process node but then outsource to a foundry the bulk of production. This is essentially the current STMicroelectronics approach and has the advantage of keeping up with technology, provided the facility is constantly upgraded for future node transitions. This

appears an elegant solution were it not for the fact a small pilot fab can never be cost-effective against a large volume fab, where it has been calculated that the minimum size to be within the top 20 most competitive fabs on manufacturing cost should be in the range of at least 30-35k (real) wafer starts per month. For a 450mm fab, this would be equivalent to a capacity of around 160k 200mm equivalent wafer starts per month.

Proponents of this route will thus face perpetual hostility from investors and the financial community asking why they are tying up capital in expensive assets and depleting shareholder value when the outsource supplier is clearly much cheaper. The only way around this is to look for the local government to help pay for every upgrade to the lab-fab and effectively subsidise the operating losses, and/or spreading the cost burden between several partners jointly operating the lab-fab as was the case of the ST/NXP/Freescale Crolles 2 Alliance. This does not however reduce the overall cost penalty in fact it might even increase it due to the added layers of bureaucracy so does nothing to address the overall scale lack of competitiveness.

The second option is to stop building fabs completely at a certain process node and then exclusively use a foundry for each subsequent process node. This is the route that e.g. Infineon and NXP have taken in Europe along with Fujitsu and Renesas in Japan and Freescale in the US. This is clearly a bipolar structure; IDM up to a certain node and then fabless thereafter. Unlike the first option, this strategy is process-terminal as, once you miss a wafer fab node, it will become virtually impossible to re-enter the wafer manufacturing business at a subsequent technology node without a lot of delay and money, if at all.

It also combines the worst of both worlds. For the legacy fabs it ignores the fundamental reality that today's leading edge is tomorrow's commodity meaning these fabs will slowly become more and more obsolete and harder to fill. There might be some scope for migrating these lines to some alternative niche technologies, like power devices or sensors that are not following the same technological route and address low volume and highly fragmented markets, but by there very nature (low volume – highly fragmented) these markets will only delay not arrest the decline. Eventually they too will need to be upgraded.

They will also be subject to constant threat from attack from fully-depreciated, more efficient, larger wafer size fabs with a far lower cost structure; a strategy used many times in the past by STMicroelectronics and more recently by TI in the power/analogue market. The real danger here will be once the 450mm transition gains momentum and the now-redundant 300mm lines seek new markets to address, they will inevitably move downstream with a more efficient and lower cost structure, squeezing the older fabs into ever smaller niches and volumes.

There is thus a real danger that these safe haven market niches and product specialties might simply end up being a stay of execution. With the exception of Dresden (GlobalFoundries and now Infineon via its recent acquisition of Qimonda's assets), Europe might well find itself wide open to attack on this front given its predominantly 200mm/150mm manufacturing base (see Chapter 8).

Europe's chip companies will thus be subjected to a constantly on-going closure and restructuring effort, damaging employee morale and affecting costs and productivity. Finding and keeping good operations personnel will be very difficult indeed given this business strategy is an operations career dead end.

The legacy overhead infrastructure, costs and inefficiency will also be much higher than with a truly fabless company and overall competitiveness will continue to erode. In short, restructuring from an IDM to a fabless business model will be challenging and unlikely to make the organisation more structurally competitive.

Aside from these issues, there is also the fundamentally unsound assumption that foundry wafers will always be cheap and freely available. This is the chip industry equivalent of the 'debt is freely available and cheap' corporate business model that came to such an abrupt and catastrophic halt in the 2007 financial crisis.

Just as with cheap debt, ever reducing prices (and profits) whilst simultaneously investing in new process and production technology cannot be sustained forever as they would lead to bankruptcy. Structurally prices must eventually increase; indeed they are already doing so.

Then there is the allocation and key account issues. Not everyone can be on the foundry's 'A'-list of accounts, which inevitably means losing control of time to market and time to revenue. The A-list customers will always receive priority, affording them a competitive market advantage. As processes become ever more standardised, so everyone will be channelled to use the same identical building blocks with no scope for process tweaking, this early technology access will be a potentially huge market advantage.

Finally, from a competitive market standpoint, if a firm like e.g. Nokia buys its next generation mobile phone chipsets from say Broadcom, Freescale, MediaTek, Qualcomm, ST-Ericson and TI who in turn then all source their wafers from TSMC, Nokia is effectively single sourced on TSMC. The whole livelihood and future of such OEM firms is thus dependent on a firm with whom they have no direct contractual agreements or commitments. Based on current plans, at the 32/28nm node, all of the other foundries, including GlobalFoundries, are currently too small in size or suffering yield problems to make a volume difference in the short to medium term, and this will only likely get worse as the technology road map rolls out.

The security of supply aftershock from the March 11, 2011 earthquake and tsunami in Japan temporarily refocused the spotlight on the strategic value of ICs (i.e. wafer production) and the fundamental perils of outsourcing and losing control of the supply chain but even this lesson has already been forgotten. Were such a catastrophe to ever hit Taiwan – itself on the same fault line – virtually the whole of the world's advance foundry SoC IC supply would grind to a halt, with no chance for any other factory to take up the slack.

These are the underlying long-term structural Fab-Lite issues. Future Horizons has long stated that the 'fab-smart' strategy remains the only true solution. This means continuing to build in-house state-of-the-art fabs while outsourcing a modest amount (say 5-15 percent maximum) to foundries to both smooth the supply and demand peaks and build external fab demand high enough to justify equipping the next module of in-house expansion. In this way any expansion in capacity enters production 'fully loaded' from the beginning whilst simultaneously improving response time to near-term demand fluctuation. The foundries do not like this option of course but this is the only real IDM competitive reality.

As already mentioned, partnering with a competitor(s) is of course another possible strategy – a scaled up version of STMicroelectronics, NXP and Freescale at Crolles 2 – to help defray the investment costs and provide additional fab loading, but this must be run and operated on best-practice foundry principles. It would require a fresh 'out-of-the-box-thinking'

operational management and investment approach, but we do not believe this is beyond the imagination of the chip making community were it mindful to so do.

Fabs have always been expensive but, as a percentage of revenue, they are relatively no more expensive today than they were in the 1970s. This basically means, to stay at the forefront of the business, firms need to keep up the pressure on sales, which in turn means a constant investment in new products. Failure to do so puts enormous pressure on cost reduction instead, which in turn triggers a slow downward spiral of cutting back on investment and R&D, the two cornerstones to future product development.

At the same time, the chip is still very much the heart of the product and downstream systems business; lose control of its manufacture and you will eventually lose control of not only your business but your customer's business as well. It is this that makes wafer processing so strategic in nature.

4.5. European Market Position

Since its peak at the end of the 1990s, when three of Europe's IDMs were in the worldwide top ten and STMicroelectronics vied for second place in the semiconductor manufacturer tables, European manufacturers have slipped inexorably downwards. Their once profitable mobile phone chipset divisions have been divested or sold off, as have the rather less profitable memory divisions, leaving them to concentrate on other so-called core competences, despite the fact that what customers – and System on Chip / System in Pacakge (SoC/SiP) devices – really need are 'one-stop shop' solutions.

STMicroelectronics still has a broad range of products and expertise but a considerable amount of this is in power, lighting control and Micro-Electro-Mechanicals (MEMs) devices, where it is the world leader, and in analogue and Microcontroller Units (MCUs), where it is near the top. None of these require the latest advanced technologies and are being successfully manufactured in Singapore, Europe and foundries. Its limited demand for mixed-signal SoCs requiring finer geometries are produced either at Crolles or its foundry partners.

Infineon has consolidated itself mainly on the Industrial and Automotive markets where it is one of the world leaders. It still has a 90nm 200mm wafer plant in Dresden, recently augmented by its recent Qimonda 300mm asset acquisition, but it is now solely reliant on foundries for its advanced logic devices.

NXP has also downsized significantly having sold off several divisions following its purchase by Private Equity. It still has staggeringly large debts and continues to be a 'restructuring work in progress'. NXP has a very long standing partnership with TSMC, who they assisted in starting up, which it uses for advanced products including a jointly owned 200mm line in Singapore (SSMC).

ST-Ericsson was formed by the consolidation of the mobile phone operations of several European companies. It is a fabless operation and we estimate that their current level of sales would fill a fab demand for around 50k 300mm wafers per month. As such, they represent the major target customer for any advanced European fab. However at this volume, which effectively fills a fab, they may be receiving very preferential terms from their current supplier(s).

Intel's mobile phone division was purchased from Infineon in 2010 and had an excellent year mainly the result of its hold on the Apple iPhone and some other key design-ins. However Intel and Apple are not always the best of friends, despite Apple changing to Intel processors in its Mac products some years ago, and the CDMA version of the iPhone4 uses a Qualcomm chipset. The success of this division depends on who has won the baseband slot in the iPhone 5 design and so it is hard to predict this group's future wafer usage.

Cambridge Silicon Radio (CSR) is the top European fabless organisation and the dominant supplier of short-range communications ICs. They are consolidating this position well with a wide range of future products essential to the wireless generation. We estimate that they currently use about 2k 300mm wafers per month which, although not fab filling, would help to load a European foundry.

There are a number of other relatively large European fabless companies, for example Icera (purchased by nVidia in May 2011) and PicoChip (purchased by MindSpeed in February 2012) but, as with Japan, Europe never really succeeded in cultivating these from the vast number of new start-ups it has spawned over the years, unlike the US and Taiwan which have both embraced this model well. This is an area that could well be improved by the presence of an advanced state-of-the-art 450mm foundry in Europe.

The research carried out as part of the Task 2 interview process, together with discussions undertaken with the Global Semiconductor Alliance (GSA), did seem to indicate, at least anecdotally, that Europe's fabless companies would benefit from the presence of a European-based 450mm fab offering foundry services. Our belief is thus that the presence of such a foundry would indeed help to develop start-up clusters across Europe, due to the easier technology access and increased share of foundry mind augmented by the considerably reduced time and cost of not having to regularly commute between Asia and Europe. We also believe that it would benefit the more integrated firms as well.

The cluster effect is discussed in more detail later but the potentially large gains in high income employment offered by new start-up companies across Europe using a European foundry is one of the major considerations that should be taken into account.

Last, but by no means least, amongst the top global European firms is ARM. It is second only to ASML in market capitalisation and profit, despite the fact that it only sells semiconductor IP. Its breadth of influence is however growing way beyond mobile devices, having now been assigned the task of developing all of the standard cell libraries for the IBM Alliance (down to at least the 11/10nm node) and have more recently started working much closer with TSMC with the implicit aim of achieving the same there. Apart from Intel with its proprietary in-house needs, this would leave ARM as the sole provider of advanced CMOS logic IC cell libraries. Thus, whilst ARM may not be directly relevant to 450mm wafers, they have now become a critical link in advanced CMOS logic design which in turn is now directly coupled to the 450mm transition.

4.6. Other European Manufacturing Strengths

The major suppliers of equipment are covered in later chapters of this Report; we just wish to point out here that Europe is a world leader in many aspects of supply to the semiconductor

industry, mostly due to hugely successful JESSI and follow-on MEDEA programmes together with European Commission supported fundamental research.

For example, ASML based in the Netherlands, supported by research at IMEC, is the world expert at semiconductor lithography. Although it is still uncertain how the 450mm transition will impact lithography technologies and equipment suppliers, ASML leadership position in advanced lithography processes is likely to be confirmed during this transition.

Europe is also the world leader at supplying Silicon On Insulator (SOI) wafers and, although Intel, Samsung and TSMC use bulk wafers, it is likely that GlobalFoundries will still offer these as a processing option given AMD and IBM both use SOI for some of their current devices. STMicroelectronics is also a user of SOI wafers at Crolles.

RECIF is one of the world leaders at robotic wafer handling and companies such as AIXTRON and ASMI (world leaders in ALD – Atomic Layer Deposition), Siltronic (bulk wafer manufacturing) and others also win business worldwide.

What all of these companies have found is that Asia now represent the majority of their sales and Europe only a very small portion. If this is not remedied then it is quite possible that more of their operations, including eventually R&D, could move to be nearer their customers. Should this happen, it would almost certainly undermine Europe's success in developing and building network clusters of excellence and be a great loss to Europe, both from a technology and job creation perspective.

We are thus of the opinion that it is crucially important to establish a 450mm manufacturing presence in Europe as a necessary condition for keeping and further developing such clusters in Europe.

4.7. Semiconductor Manufacturing Conclusions

The situation for the European manufacture of advanced CMOS logic semiconductors is not very good. Current own-produced volumes are low (STMicroelectronics) or non-existent (Infineon and NXP) made worse by the fact that, whilst STMicroelectronics is still one of the few remaining broad range supply firms worldwide, together with Renesas and a lesser extent TI, even these companies are driving to streamline and concentrate on their perceived market strengths. This will inevitably have an effect on the type of semiconductors they produce and, if these are not at the most advanced technology nodes, there is less justification in paying for or using a state-of-the-art 450mm wafer fab.

That said, STMicroelectronics still has the need for advanced wafer production, for example for its range of Set-Top-Box and networking products, but its current run-rate means it cannot fill an economically sized 450mm plant. It is also not profitable enough to generate the cash needed to build a full-scale 450mm wafer fab.

Infineon has a similar but more focused strategy and probably less need for the most advanced geometries. Its requirements are more for devices with on-board communication and volatile/non-volatile memory to produce truly single chip systems for its target market. We believe such devices are just moving to the 65nm node so the inherent lag in these products makes access to a state-of-the-art 450mm fab plant less important. However they will require access to such a plant once it is amortised and behind the state-of-the-art node.

Unfortunately at the moment the use of Far Eastern foundries does appear the best way to achieve this, although GlobalFoundries may present an alternative in the future.

NXP does have some product lines that require state-of-the-art nodes but their long-standing relationship with TSMC might be a huge barrier to entry for a new European-based fab, given that it might not, at first glance, seem to be in NXP's best interested to risk potentially damaging this long history of co-operation. However, looking at it from a purely financial perspective, whereas NXP needs TSMC, it could be argued that TSMC does not necessarily need NXP, so the presence of a 450mm foundry in Europe might also be to NXP's strategic advantage.

For the time-being, ST-Ericsson still has the potential to achieve a successful re-organisation and remain one of the top-tier players in the mobile chipset market, together with Qualcomm, Broadcom and MediaTek, with a few second-tier players left to exploit some niche areas. The mobile chipset market remains huge and in the future, with the move to 4G, Qualcomm may have less of a stranglehold upon it. Provided ST-Ericsson can win key design-ins then they will continue to need huge numbers of wafers at the most advanced technologies but it has to be said its time is running out. It is also hugely loss-making which severely limits its options.

Beyond these, there are a number of smaller fabless companies who could also use a European 450mm fab if it offered foundry services and was fitted to economically process small to medium-volume orders. Such availability could also assist in unlocking investment capital for other start-ups who are currently not winning investment due to issues such as tight lead-edge wafer capacity, meaning they will never have early access to state-of-the-art advanced CMOS processes. This would need to be offered and staffed accordingly in a way that was cost-effective for the foundry otherwise it would negatively impact the overall 450mm project but, with a fresh open box approach, as with the co-owned option, we do not see this as a major barrier to overcome. Access could be readily co-ordinated and sold via existing European programmes such as Europractice.

Taking all of these factors into account, it would seem reasonable to conclude that there was sufficient need and market demand to support at least one high-volume, state-of-the-art 450mm wafer fab in Europe provided it offers foundry services both to Europe's fabless community and the indigenous IDMs. It can only be justified however if sufficient charter key European companies were committed to its success. Once established we believe such a fab would also prove attractive to the leading global fabless (Broadcom, nVidea and Qualcomm etc) and fab-lite (Freescale and Renesas etc) firms, thereby enhancing its cost structure and economic feasibility.

Looking at the broader agenda, there is also the possibility to persuade one of the top three 450mm pioneers (Intel, Samsung and TSMC) to set up a 450mm fab in Europe, capitalising on the rich European 450mm advanced R&D and cluster infrastructure. This might also open the door for GlobalFoundries to participate earlier than they might otherwise have been able to, and every effort must be expended to ensure that all potential locations, especially Leixlip and Dresden – Europe's two most advanced manufacturing centres – remain favourable places for chip companies to operate in.

Given Europe's commitment to developing and keeping advanced manufacturing in Europe, whatever strategy is eventually adopted, it will need to ensure that Europe remains a

competitive place for its equipment and materials manufacturers and advanced research institutes to operate in, even if the bulk of their business resides in the Far East.

In addition to this opportunity, we further believe that there is a parallel opportunity for a European-based 450mm wafer fab focused on more mature technology node processing. Whilst this may at first glance sound like a nonsensical idea, especially as 450mm and advance-state-of-the-art processing have become de-facto synonymous, it would actually help both de-risk the 450mm transition – by providing a platform to run proven technologies for a much longer period of time envisaged by the current state-of-the-art 450mm roll out on – and provide an advanced, lower-cost manufacturing platform for Europe's MtM-based technologies.

The fab would need to be designed and built 'future-proof', in order to avoid building a blind alley, which in essence means designing it to be a high-volume state-of-the-art MM fab but initially only equipping it with the equipment and facilities needed for lower technology node MtM production. For example, this would mean making sure that the fab can accommodate the advanced EUV and immersion lithography needed for sub-65nm production, but housed in an adjoining building Annex so that this part of the facility does not need to be constructed at the start of the project.

The lower processing complexity would also mean less equipment was required for the main wafer fab but this too would be built to accommodate complexity expansion over time. On starting up therefore, the fab would be equipped with 450mm tools required to process 65nm and higher structures. This toolset would then be gradually updated to accommodate more advanced process and state-of-the-art nodes in due times.

We further believe that there is collectively enough production volume to fill such a large-volume fab, given the majority of Europe's current production at these nodes is in older, 150nm and 200mm fabs, all of which need expanding and/or upgrading within the next five years, i.e. the timescale of this project.

Consolidating this into a single 450mm fab would bring huge benefits in production efficiency, technology capability and die cost reduction. The yields, scale and efficiency of the resultant production will be significantly better that those for its competitors, even if on a fully depreciated 300mm line, giving Europe's MtM chip firms a huge market advantage…a unique European win-win scenario.

There would also be benefits to the equipment industry and Europe's research facilities by helping to engineer solutions to the 450mm-wafer size related problems, using even more well-established nodes over a much longer period of time and allowing MtM technologies to be developed on a 450mm platform much earlier than would otherwise be possible.

This option is discussed in more detail later on in the Report (see Chapter 17).

5. The 450mm Bifurcation

The purpose of the following chapters is to provide the reader with an overview of the 450mm transition process and its anticipated impact on the SC supply chain. A timescale for the 450mm transition is also provided based on early adopters' announcements and industry's readiness level.

5.1. 450mm Rollout Scenario

There are still some dissenting opinions as to whether the semiconductor process node road map and the transition to 450mm wafers are independent topics or if the two will need to become intrinsically linked. This is complicated by the fact that the technology roadmap, from today's 32/28nm advanced production node to the 11/10nm structures we can expect to see in early production around 2015, are littered with process dislocations, both in the structure of the transistors and the means to pattern and build them.

One of the lessons to be learnt from the 300mm conversion was that the two issues were initially isolated, meaning that the conversion node became a moving target, starting off at 250nm, ultimately ending up as 90nm, causing a raft of false starts, overlapping and redundant equipment development costs. It is this 'wasted' R&D spend that bruised the equipment industry so badly, hence their reluctance to readily embrace the 450mm transition.

Whatever the conclusion of this debate, consultations across the SC industry confirmed that the 450mm rollout must and will be better coordinated across the supply chain as already shown by the G450 Consortium in Albany formalized and publicly announced on September 27th 2011. In our opinion three things are becoming clear:

- The first pilot production 450mm wafers will be on a proven (n-1) high-volume production process and mature chip design in order to run-in, match and then (hopefully) exceed all of the measurable 300mm process performance characteristics

- Once process and platform stability has been achieved (one year?), the process technology will flip to the then current leading edge node resulting in parallel chip production on 300mm and 450mm lines, during which time 450mm development will be focused on yield, cost improvement and production volume ramp-up

- Once cost parity has been achieved (or in sight), production will immediately flip to 450mm only with 300mm phasing over to less demanding application areas, such as chip sets, controllers and more mature SoC ICs

5.2. SC Industry At A Cross-Roads

At the time of introduction, and for the first year of operation, 300mm fabs will be operating at a more advanced node than early 450mm fabs and 450mm produced die will likely carry a cost penalty compared to their 300mm fabbed counterparts.

However, once parity has been reached, the cost benefits will start to gain traction and, for those firms on a 450mm platform from that point on all future advanced-node development across their entire product range will be solely on the 450mm platform. Existing 300mm production capacity at that node will be either progressively phased out and the equipment sold on, or turned to other less demanding areas, for example to cost reduce 200mm-based products.

For these firms 300mm capacity expansion will be focused on process improvements limited to implementing best practice and/or improved processing techniques stolen from their 450mm experience wherever this is practical, as with e.g. CMP at the 200mm size. This will leave the equipment industry with limited R&D resources and dwindling long-term 300mm demand to focus solely on 450mm. It only takes one firm to drop 300mm support at the state-of-the-art for it to be impossible for a complete state-of-the-art 300mm fab to be built.

This bifurcating moment for the semiconductor industry has been confirmed during Task 2 interviews indicating that once 450mm enters full-scale production, further 300mm node development will cease for equipment suppliers due to the following reasons:

- Equipment industry will have limited resources and concentrate on the largest share of the market providing the largest Return on Investment. At the time of the transition, between 60-75 percent of the Capital Expenses (Cap Ex) dollars will be driven 450mm demand from the world's chip market gorillas, with the residual, and declining, Cap Ex coming from the rest of the industry

- 450mm platforms will be more competitive from a chip manufacturer's cost perspective and common platform / body 'proposal' capable of processing both 300mm and 450mm wafers will not be economically viable for a vast majority of equipment suppliers (about the same cost but only half the throughput)

Following the wafer scale-up, future node development will rapidly occur only on the 450mm platform, although there will of course still be further developments on larger nodes on the 300mm platform under the MtM concept.

Faced with competitive pressure from their 450mm-based competitors, the only course of action for 300mm fabs will be to (a) somehow address their upgrade path to 450mm, either by becoming 100 percent fabless at these process nodes (by then the so-called 'fab-lite' model will not be an option); (b) merge and/or form production joint ventures; (c) continue to face slow death by competitive market strangulation; or (d) exit these markets and move into other niches and/or specialty product, in much the same way as Europe's chip firms did at the 300mm/65nm node.

This latter group of firms will thus be joining what will be an increasingly overcrowded market as more and more competitors are forced into market niches and speciality products both of which are, by definition, relatively small and diverse. To make matters worse, whilst it may well be the case that their advanced technology base is still at least 1-2 nodes behind the leading edge, meaning they will likely have at least 2-3 nodes 'in the bag' yet to embrace, within 5-6 years from transition they will find that the only place they can get their base technology from will be a 450mm platform. They too will de facto become fabless, other than for legacy products.

In the near-term the issue is somewhat irrelevant; the two wafer sizes will be co-developed, meaning all next generation 300mm equipment will be developed with 450mm features and requirements in mind. The first generation 450mm fab production (pilot) line equipment will be process robust and production fab ready, as opposed to the 'throw-away' early test wafer and demo tools, albeit not yet optimised for performance and throughput. These tools will be capable of operating at the then most advanced node, exactly in synch with their 300mm counterparts. They will not however start production at this node.

5.3. Early 450mm Entrants & Products

The first 300mm pilot lines took almost a year to achieve comparable yields with 200mm wafers and there is no reason to believe things will be any different with 450mm. Thus the early 450mm adopters will have to manage this changeover period when finished die from a 450mm fab will actually cost more than those from a 300mm fab.

Once the pilot line is at acceptable yields, it will then be necessary to equip the rest of the fab to achieve full capacity. Even assuming the necessary processing equipment is available, possibly due to an advance ordering mechanism similar to the manner civil aircraft are ordered, it will still take a further two years for the early volumes fab to reach full production.

5.3.1. Intel

Intel is the prime driver in the move to 450mm wafer processing and they have stated their intent to run in the first line on a proven process/IC design combination at the 15nm node before moving to 11nm once everything is proven capable of operating at this node properly. Although any new line is debugged first using test chips, being already in mass manufacture of the same part on their 300mm lines provides a perfect reference to allow them to optimise the new equipment and process flow.

Intel has a different cost structure to almost every other company in the industry in that their fabs are less sensitive to cost optimization, nor really are their designs. They rely on using the most advanced technologies to deliver the highest computing power on the market, which they can then sell at a premium price and profit margin. Given that they will be in parallel production on both lines, we expect that they will simply amortise the cost differences internally making it difficult for outsiders to learn the real costs of the transition.

There have been some tacit moves by Intel towards manufacturing for other companies but these have always been in high-end niche products requiring the unique speeds of their proprietary processes. We do not expect this to change in the near future although with their Tri-Gate process the combination of a lower power process might open the door to Intel adopting a foundry business model targeted at the large, advanced mobile SoC logic market for the top tier OEM accounts such as Apple, Cisco, EMC, Juniper, Motorola, Nokia and Sony. They have made it quite clear though that ARM processors are unlikely to be offered in this manner. If this did happen on early 450mm manufacturing platforms it would be a game-changing market disruption but we expect that they will concentrate such production on their own processors until they have two or probably three 450mm fabs in operation.

5.3.2. TSMC

TSMC has the most efficient fab management in the world and claims to be still profitable when running at around 45 percent of capacity. Much of this is due to the sheer scale of their operations compared with their competitors. Their new 'Giga-Fabs' will further consolidate this advantage. It will be interesting to see how they allocate wafers on their first 450mm fab and how much they charge for them.

TSMC is perhaps the most complicated 450mm business case given that its first 450mm product will have to be a logic IC. The key decision will therefore be whether the first 450mm process will be their high-speed or low-power options. Although there is not a great difference between the two flows, one will take priority as they will not want to be reconfiguring equipment repeatedly during the initial calibration and pilot run phase.

An interesting discussion occurred at a forum in summer 2011 when somebody pointed out that the company most able to afford a 450mm fab was Qualcomm. They currently use TSMC as their sole fab source and although there has been no comment from Qualcomm or TSMC, the possibility that Qualcomm could purchase the complete output of their first 450mm fab in advance does raise interesting scenarios for the rest of the fabless industry.

Whatever the outcome, it is clear that the bulk of TSMC's customers will continue to be sourced from 300mm fabs for at least one to two more process generations after the switch, potentially alienating some very large customers.

5.3.3. Samsung

Samsung is a little different as they have memory (DRAM + Flash) and logic processes, the latter being available for both its in-house and foundry customers. They too have a different cost model but are believed to have a significant cost advantage over others in the memory market. The foundry activities of this company are actually quite small, being restricted to just a few key high-value clients to complement their own much larger internal needs. They are therefore less exposed to the risk of a pure-play foundry logic fab not being fully utilised.

A memory orientated fab has a much simpler process flow and higher per design IC production volumes, combined with the error correction techniques designed into all current memory designs means it could have the fastest time to a marketable product. Flash might also have an advantage over DRAM given that it does not necessarily require EUV processing but is instead moving to stacked transistors to obtain greater density.

We therefore expect that their first 450mm fab will be a memory fab, the only uncertainty being whether this would be DRAM or Flash. Already the world's top DRAM and (jointly with Toshiba) Flash memory supplier, once yields settled down, a 450mm cost structure would consolidate their position as THE world dominant memory manufacturer.

5.4. Follow-On 450mm Entrants

Whatever the eventual 450mm rollout, one thing is clear. Once on a 450mm platform, Intel, Samsung and TSMC, with combined 'as sold' market revenues of around US$100 billion in

2011 (~42 percent of the total IC market), will have a sizeable competitive advantage over the rest of the industry. They would totally dominate the MPU (Intel does already), memory (Samsung is already the market leader) and SoC/Logic (where TSMC dominates) markets.

Memories would be the first to feel the cost advantage pain, closely followed by the foundry market, both sectors of which, Samsung and TSMC aside, are already barely profitable. Toshiba and GlobalFoundries, given their current strong 300mm positions, have the most to lose but anyone competing against Samsung and TSMC's 450mm cost structure on similar product categories will be driven into profitless oblivion.

The IBM Common Platform Alliance would also be at risk on a 300mm cost platform. Their position has already been compromised by their decision to bet the wrong horse and promote Gate-First technology at 32nm, with the difficulties in bringing up volume production at this node now impacting on the engineering resources and early wafer availability for their 22/20nm Gate-Last technology, potentially impacting the competitive position of the IBM Alliance partners.

The firms (products) we believe to be most at risk from Intel (MPU), Samsung (DRAM & Flash) and TSMC's (Logic/SoC) move to 450mm are thus Toshiba (Flash), GlobalFoundries (Logic/SoC) and IBM (Common Platform Alliance), followed by the other top memory, foundry suppliers and the remaining IDMs, Figure 4.

Figure 4 – Current & Potential 450mm Adopters
(In Alphabetical Order)

Early Adopters	Potential Eventual Players
Intel	Elpida
Samsung	GlobalFoundries
TSMC	Hynix
	IBM
	IMFlash
	Micron
	Nanya/Inotera
	Powerchip
	ProMOS
	Renesas
	SMIC
	STMicroelectronics
	Toshiba
	UMC

Source: Future Horizons

Not all of the 14 potential players will decide (or be able) to build a 450mm fab but already two recently announced fast followers (GlobalFoundries and IBM) are more than just waiting in the wings. As for the others, the transition may well trigger a raft of industry consolidation, especially in the memory arena where most firms just simply do not have sufficient cash. It is also quite possible that political pressure will come into play once countries start to realise that their 'national champions' are on the ropes.

Overall we expect that the final number of companies able to build 450mm fabs might just scrape into double digits at 10.

5.5. 450mm Transition Timing

5.5.1. Semiconductor Roadmap Influence On 450mm Transition?

Chapter 6 provides a detailed overview of the forthcoming semiconductor technological roadmap during which the transition to 450mm will occur and particularly highlights the three major trends and challenges faced by the SC industry in this decade:

- Unclear and complex process technology roadmap for advanced CMOS transistors
- Transition to next generation patterning techniques and more particularly EUV
- 3D heterogeneous integration technologies

At the start of this assignment, there were lots of uncertainties as to whether these challenges will delay the transition to 450mm wafers due to technological, financial and/or strategic reasons. EUV lithography was in particular regularly pointed out as being a key enabler for the transition to 450mm.

Internal researches and consultations have clearly indicated that, from a technological perspective, the 450mm transition is totally independent from the above-mentioned challenges for the following reasons:

- Foreseeable transistor architectures are not wafer-size dependent
- 450mm production will happen with or without EUV since it will bring cost reduction compared to 300mm platforms for any given lithography process
- Although 450mm wafer might bring some additional challenges to some 3D techniques due to the increased thickness of wafers, it only concerns a subset of the 450mm market and 450mm dies will anyway provide a competitive advantage to such assemblies compared to pure-300mm 3D integration

From a financial perspective, such a convergence of issues will undoubtedly require further considerable private investment and public support for the appropriate research and industry

cooperation. As already mentioned, priorities will vary from one player to another depending on product portfolios, financial resources and corporate strategies, leading to different 450mm transition dates at the company level.

5.5.2. 450mm Manufacturing Introduction Dates

As mentioned earlier, we believe that the first 450mm production wafers will be at node n-1 but they will be flipped to node n just as soon as the 450mm platform bugs are ironed out with comparable or better wafer fab yields and performance to established past-practice. This might be sooner rather than later for Intel, given its high-performance-based fab business model, and later rather than sooner for TSMC, where stable yields and low cost are the key driving factors, although we expect a few fabless semiconductor firms would be prepared to share the potential die cost risk with TSMC in order to benefit from the early 450mm experience. Samsung's roll out is much harder to predict, especially as it will be strongly influenced by whether the first parts are DRAM, NAND Flash or even SoC logic.

Intel has stated that their first 450mm pilot plant will be at Hillsboro in Oregon in their new D1X fab and that this will be used to debug the production process before moving it to other high-volume sites. Currently this fab is in very early construction, planned for a 300mm line initially and a 450mm pilot line sometime thereafter.

The second plant will be in Arizona which leaves the location of the third plant to be decided. This could be in the US, Israel or Ireland. Although we obviously were not privy to the confidential discussions, we gained the impression that strong lobbying from Ireland is already taking place for Leixlip to be named as Intel's third 450mm fab. Leixlip's proximity to ASML and IMEC should in theory give it an advantage over e.g. Israel.

TSMC originally made a statement that their first 450mm pilot line was planned for their Fab 12 Phase 6, starting with 20nm technology. The timing of this pilot line is said to be 2013-14, with 450mm production line planned for 2015-16. If met, this timescale would be 1-2 years more aggressive than Intel and we believe the dates to be more PR than factual. It is known though that their 20nm process is well advanced with ARM building a Cortex A-15 chip to prove both the TSMC process and ARM's cell library at this node.

Samsung, on the other hand, has made no public 450mm announcements on either the locations or timescales for its 450mm plans and, given the cost effectiveness of its 300mm lines, it may be that they will wait for the others to make the initial 450mm moves first.

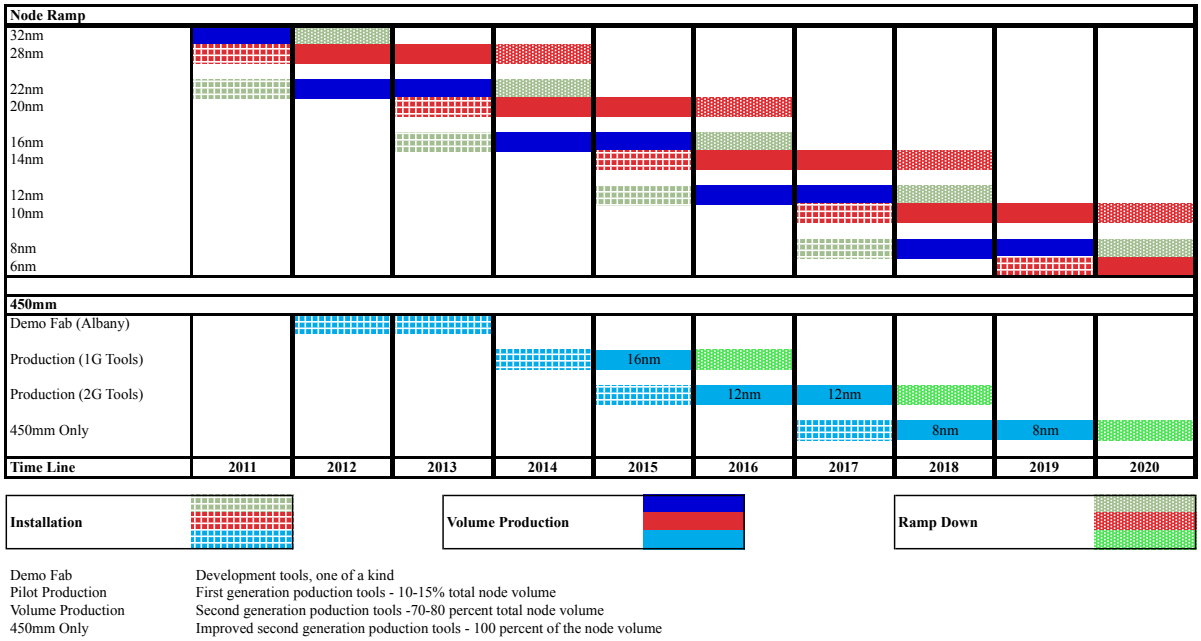
At the practical level, to date the most actual work has been done at Sematech's ISMI subsidiary in Austin, Texas and by IMEC in Leuven with the effort now moving from wafer handling infrastructure to early wafer processing. Given the uncertainty over the production introduction, progress to date has been slow but with this uncertainty now removed, we can expect to see an acceleration of this progress. This began with the relocation of ISMI to Albany followed by a host of announcements culminating in the Global 450 Consortium (G450C) being established. Intel has unofficially said that membership of this is compulsory for any equipment or material manufacturer wishing to supply them and so Albany definitely now has traction over IMEC in this field.

As for the timing, even if efforts were stepped up considerably, it is now impossible that the first fully working 450mm pilot fab equipped with first generation equipment could be built before 2015.

5.5.3. Best-Case Rollout Timing

The 450mm technology road map will be driven by the current 300mm advanced technologies roadmap, despite the fact its early production life will start one or two generations in arrears. Based on this model, the best-case roll out timing would imply early test tools in 2012, demo tools in 2012-13, with first generation production tools available in 2015. This would place the 450mm transition node at 11nm, with initial production at 16nm. The technology wall of death for the remaining 300mm-base producers would start to bite home in the 2020 time frame, Figure 5. For the 200mm-base manufacturers, five years earlier in 2015.

Figure 5 – Best Case 450mm Rollout Timing



Demo Fab	Development tools, one of a kind
Pilot Production	First generation poduction tools - 10-15% total node volume
Volume Production	Second generation poduction tools -70-80 percent total node volume
450mm Only	Improved second generation poduction tools - 100 percent of the node volume

5.6. Summary & Conclusions

The 450mm will and is already a major disruption for the semiconductor industry, triggering a new wave of consolidation and a clear bifurcation between the suppliers of equipment and material but also the chip suppliers. 450mm will set a new cost structure for the industry with subsequent impacts on the competitive landscape with different timeframe depending on the technology considered. Based on current best-case transition timing scenario, 200mm

manufacturing base will first be put under pressure before the end of the decade while 300mm industrial base will start declining five years later.

Another thing that is clear is the need for the platform transition roadmap to be much better co-ordinated across the full industry spectrum. The G450C cluster, together with the SEMATECH, EEMI450 and other initiatives (IMEC) have already gone a long way to co-ordinating these efforts, supported by informal discussions between the major interested parties. This will undoubtedly result in a much better orchestrated transition than has ever been previously achieved; it needs to, the financial and technology risks are too high. Much effort is thus being extended to get the transition right; whatever decisions are taken now with haunt the industry for the next 20 years.

With all of the above factors in mind, we believe that the time is right for a different industry business model, adopting best practice from similar high R&D cost industries, such as the aircraft industry, whereby these costs are shared by all of the parties involved with the possible support of PAs, both by matched R&D grants, financial incentives, 'guaranteed' loans and other financial instruments together with much greater clarity of demand with real call-out commitments, supported by deposits and cancellation penalties, as opposed to today's laissez faire, boom to bust, free market norm.

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6. Semiconductor Technology & Processes

Over the past decade or so, CMOS IC design has become highly segmented with most designers becoming well isolated from the actual silicon. Huge blocks of pre-designed IP can be assembled on a chip meaning that designers often also have little contact with many of the actual gates and transistors, this being left to the IP providers and standard cell and IP block design experts such as ARM and Synopsys.

As transistor sizes shrink ever smaller, we begin to reach atomic limits whereby probability and quantum physics must be taken into account, not just at the transistor level but also at higher levels. This is known as the post-CMOS era and is expected to impact below the 8nm node. This transition will herald one of the biggest design and manufacturing methodology changes that the industry has ever faced. Everything, from transistor structures through design tools, system and circuit design and even embedded software, will dramatically change.

On current timescales, this change will impact not long after the introduction of 450mm wafer processing. Should, as seems likely, the 450mm transition confine all future node development work to be exclusively on the 450mm platform, the post-CMOS transition to future structures will also happen exclusively on 450mm wafers.

Without access to suitable processing for the post-CMOS era, Europe would not be able to maintain expertise in leading-edge IC production and this would have critical effects not only on the indigenous IC industry and research labs but also downstream on the value chain for both the existing industrial sectors that rely on advanced semiconductor technologies and the ones that are still to develop.

The following sections thus detail some of the issues involved in maintaining this expertise and provide the reader with an overview of the forthcoming technological roadmap over the next decade during which the transition will be made from 300mm wafer processing to exclusively 450mm wafer processing at the leading edge technologies.

6.1. Technology Nodes & Players' Positions

Semiconductor technology advances through what are called nodes, which are named by the length of the smallest gates in that technology. In the past the process node steps and names were all well agreed; 180nm, 150nm, 130nm, 90nm and 65nm being examples, with the naming of these nodes being part of the ITRS roadmap. This line width reduction and therefore transistor area shrinkage, is often referred to as Moore's Law although this is not strictly correct. Moore's law postulated an increase in processing power; the industry simply used transistor shrinking as the easy means to achieve this, resulting in the two issues becoming synonymous.

Whilst the roadmap still lists future nodes and dates in its documentation, for example 22nm in 2011, 16nm in 2013, 11nm in 2016 and 8nm in 2019, several key companies have recently diverged from these names, possibly for commercial reasons, initially citing these as interim 'half-nodes' before subsequently announcing their intent to jump directly to the half-node. For example we see 32nm/28nm and 22nm/20nm used, whilst the next node is regularly stated as 16/14nm.

The terminology used in this Report tends to reflect both the node name given by the company being discussed and the ITRS roadmap name, however it should be noted that there is probably little, if any, technical difference between the different node names and most companies will in essence achieve very similar densities, these diverging only gradually as the transistors and standard cells are optimised over the node lifetime.

Intel has brought their 22nm process to full production at several of its fabs, including a recent investment of US$2.7 billion in Israel to upgrade this fab to utilise this process on 300mm wafers.

In memories, Elpida have announced a 25nm step DRAM whilst several Flash NAND suppliers are beginning to ship around this node. It should be noted though that memory nodes are different to logic and MPU nodes and so the numbers quoted are not exactly equivalent.

In logic, all other companies are currently around two years behind Intel, with several still struggling to get the 32nm/28nm step to yield acceptably. TSMC appears to have solved most of the problems with their hi-k gate process but there are still stories of some customers having yield problems whilst others, such as Altera and Xilinx, are yielding very well. Similarly GlobalFoundries has been having yield and delay problems that have been well publicised for some time now and is causing major problems for their prime customer AMD.

The IBM Common Platform Alliance's choice of gate-first technology for the 32/28nm node has also made it more difficult for the Alliance to evolve to the gate last technology needed at 22/20nm. Despite this, the Alliance is claiming 20nm in 2012, 14nm in 2014 and 11nm/10nm in 2016. TSMC is also making similar claims and might just have the timing advantage.

We believe that GlobalFoundries, Samsung and TSMC are all laying out test chips using the same ARM A15 processor but optimised for their own 20nm transistor designs. Provided these designs all function as expected, the ARM designed cell libraries from these will then be distributed to key Tier 1 customers towards the end of 2012 leading to risk production of the Alliance 20nm beginning in 2014 with full production towards the end of the same year.

Further ahead we are aware of problems with the currently foreseen EDA toolsets at the 14nm node and so further delays can be expected for these suppliers. Intel has its own internal toolset development and so will not suffer these delays and we expect their 14nm process to be announced at the end of 2012/early 2013 entering full production in 2014.

We then expect the divergence between Intel and the rest of the industry to increase over the next few process nodes, given Intel's proven ability to make each process transition work to schedule. Even so, it is reasonable to expect even Intel to struggle to keep to a 2-year Moore's Law cycle and we expect a 3-year cycle will become the norm for them and the top memory companies.

6.2. Process Development Costs

Keeping to the node shrinking timing of Moore's Law imposes massive technical and funding challenges on process development. The current 22nm node cost around US$1.5 billion for each company or alliance to develop, whilst 15nm and 11/10nm will cost around US$2.2

billion and US$3.0 billion respectively, coming in addition to the cost of equipping fabs to utilise the process. It is accepted that few companies can afford these sums on their own.

Even Intel utilises some shared front-end research at IMEC, whilst Samsung, IBM, STMicroelectronics, Global Foundries and others have fairly compatible processes at the GDS-II level and so can share much of the process development costs. These costs will have to be incurred whatever the wafer size and are therefore wafer size neutral.

As 450mm wafers are inherently more expensive to produce, it makes little sense to run the huge numbers of test wafers required at this size if suitable 300mm processing equipment is available. This in turn will mean that pilot and early production will also be on 300mm equipment whilst the process is transferred to the 450mm fab.

We thus anticipate all early production up to and including the 8nm node will take place on 300mm wafers first, transferring to more expensive 450mm wafer processing only once the process is optimised and yielding well. This does not mean that production quantities will be produced on 300mm but that development and customer samples will use this wafer size.

However this strategy will not be possible at 5nm (possibly even 8nm) which will thus become the first node where all development, testing, pilot and full production will take place only on 450mm wafers simply due to the lack of development of suitable processing equipment at the 300mm wafer size. We expect Intel to demonstrate their 5nm process in 2020 and move it to full production in 2022, with TSMC's variant of this node reaching full production around 2025.

6.3. Process Technology Challenges & Roadmap

6.3.1. Current Process Technology

Each new process below 100nm has required a major innovation to maintain transistor performance, specifically to keep the leakage current low enough for there to be both an adequate ratio between the on and off current for the device and to keep the power consumption of the IC at reasonable levels.

Intel introduced hafnium-based hi-k gates at 45nm, although others chose to remain with planar silicon gate transistors and reduce leakage by other means. At the 32nm node, hi-k metal gate became the accepted technique across the industry, but with Intel, Samsung and TSMC staying with standard silicon wafers, whilst IBM and GlobalFoundries continued with their well established SOI approach.

Meanwhile the memory companies also introduced more exotic processing techniques which split the industry, with the smaller players stuck at around the 48nm node or larger and the bigger players moving into the 3x nm and 2x nm nodes.

For logic at the 22nm node, current hi-k gates are not good enough to contain the leakage due to the drain induced barrier lowering (DIBL) effects causing the transistor to pass electrons independently of the gate. There are four solutions to this, namely:

- Continue with the planar process but with improved single gate and channel material given there are now better hi-k gate materials and structures available for these second and third generation hi-k gates

- Adopt a dual gate planar approach whereby a second gate is diffused below the channel, matching the one above. The ability to control the channel from both sides significantly reduces leakage. The back-gate does not need to be as tightly coupled to the channel as it is used purely to reduce leakage, not to create fast switching

- Move to 3D structure such as the FinFET or Tri-Gate, using a raised gate channel on a bulk substrate, thereby allowing the multi-finned gate to control three of the four sides of the channel and thereby counteract the effects of the drain field even more effectively. However the downside is that the structure becomes far more complicated than planar processes

- Make the channel thinner and directly isolate the underside of it with the oxide layer of an SOI wafer, thereby preventing any current flow in areas distant from the gate. This is known as the ultra-thin body (UTB) device, often referred to as fully depleted silicon on insulator (FD-SOI)

A key advantage of the last two options is that the channel can be lightly doped or preferably undoped, with the n- and p-channel operation created by the gate, source and drain biasing structures. This is known as fully depleted operation and gives a significantly reduced 'off' current and a lower threshold voltage required to turn the transistor on. Both of these can reduce supply current significantly and the gain is estimated to be at least 33 percent over the planar solution. Another advantage of an undoped channel is that this removes one of the main sources of transistor variance and so the transistors operate nearer their expected operating parameters and smaller guard-bands need to be included in the cell libraries.

Arguments over whether FinFET or FD-SOI is better tend to get rather emotional. In practice the performance of each can be expected to be fairly similar with the choice coming down to the cost of the extra processing steps required for the 3D structure against that of the special SOI wafers required for FD-SOI.

Most companies have evaluated all of these structures in their R&D labs, with Intel opting for a FinFET solution at 22nm, whilst TSMC and the Common Platform Alliance have decided they can squeeze one more node out of planar using third generation hi-k gates and so are remaining with this at 20nm.

Meanwhile STMicroelectonics is known to be seeking funding to pursue an FD-SOI development at this node. ARM has been looking at FinFET on SOI and FD-SOI technologies carefully and evaluating how it will affect their cell libraries, but at the current time they only have very small teams dealing at these technologies with most effort going on planar on bulk and planar on SOI technologies, as required by their key customers at the 20nm node.

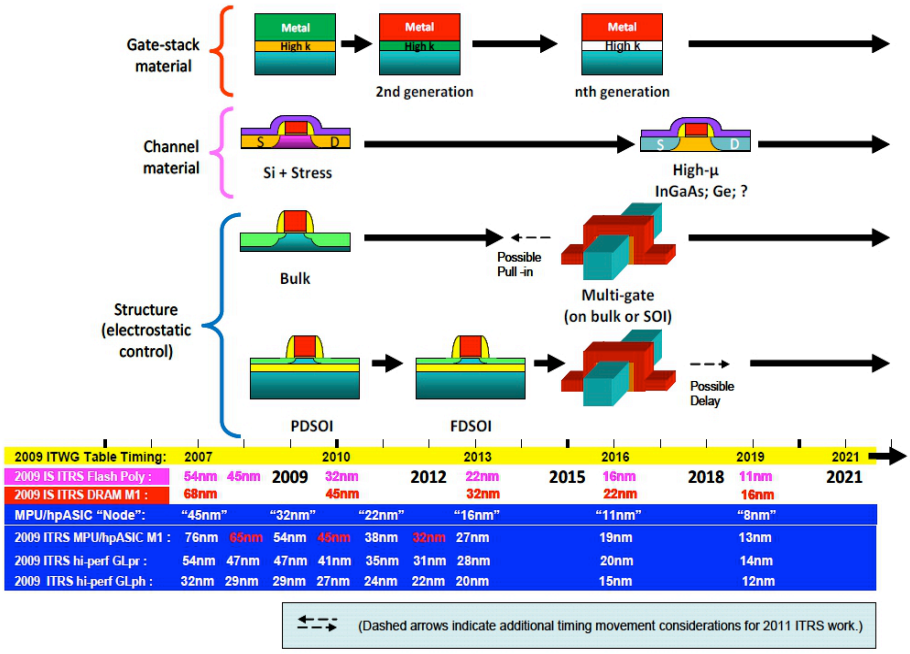
6.3.2. 14/15/16nm Process Technology

Figure 6 below summarises the ITRS ORTC (Overall Roadmap Technology Characteristics) including an overlay of the 2009 industry logic nodes and ITRS trends for comparison for 2009 through 2021 but the later dates should be seen as very approximate.

Since this graph was first published, it has become obvious that the Multi-gate method on bulk has indeed pulled-in whilst the FD-SOI approach has been delayed by at least a generation. Also the third generation of hi-k gate materials are currently entering production.

When we began writing this Report, this figure could still be viewed as fairly accurate. Although less accurate now, we are still including it because there is not a more up to date one available and it indicates the breakneck speed at which the chip industry moves.

Figure 6 – ORTC Graph Of Trends



Source: ITRS (2011)

Compared with the 20/22nm step, at 16nm the technical issues become even more complicated. Intel will of course continue with their TriGate devices but it is possible that they will introduce high-mobility channels, at least for the highest performing variant of their process. For the p-device, a SiGe channel could be used whilst for the n-device one possibility is for a channel made of III-V material. Although Intel evaluates all options and is a key member of the SOI450 consortium (cooperative R&D project labelled by the CATRENE Eureka cluster), production at 14nm is already committed to be on bulk wafers.

Although TSMC will be unable to put off using FinFETs at 14nm, we expect they will avoid these new channel materials for one extra node when compared with Intel. Quite what TSMC have planned is unclear but it is reasonable to assume they will also remain with bulk wafers at this node.

For the Alliance, IBM's roadmaps state their 14nm step as being 'FinFET on SOI' but we are aware they are evaluating an UTBB (Ultra Thin Body and Box) approach on SOI wafers. UTBB is an evolution of FD-SOI and either at this node or the following it will gain a second gate diffused below the oxide layer of the SOI wafer. It is thus inherently more complex than current FD-SOI but does give the transistor similar 'off' current to a vertically fabricated 3D device.

At the 2011 Nanoelectronics Forum in Ireland, Gilles Thomas of STMicroelectronics, when presenting the results of the DECISIF project, stated that in fact at this point the competing processes converge, with UTBB being a FinFET transistor turned on its side or a vice versa.

In practice we expect the Alliance to continue with both approaches currently in development and a decision will be taken during 2013 on which one to take to production.

6.3.3. Future Process Technologies

At the 11nm node further improvements will be needed to the channel material. Since the SiGe and III-V gate materials are deposited on the wafer as part of the production process will not be completely homogeneous. Thus the variance of the channel will become a serious obstacle to production and the guard bands on cell libraries will have to be significantly wider, thereby removing some of the advantages of moving to smaller nodes.

One possibility to reduce this problem is the use of molybdenite (molybdenum disulphide) as the channel material but there will of course be many improvements to the deposition of the SiGe and III-V materials which may remove the need for another change in material.

It should be noted that all of these channels are created by deposition on standard or SOI wafers so at least there will be no major new processing equipment or techniques required. However the number of machines required will be increased as, for cross contamination reasons, they each need to be dedicated to one material only.

At the 11/10nm node we can expect Intel to add local insulation and a back-gate below a 3D structure on bulk silicon. This is termed LSOI (localised Silicon on Insulator) and could potentially also be the structure used for SRAMs at 14nm. Although LSOI is more complicated than UTBB, the processing cost is offset by the higher cost of SOI wafers and it remains to be seen which will prove to be the best choice. It is thus necessary to ensure solutions for both approaches are production-ready and Intel is believed to be following this strategy.

At the 8nm node we begin to reach the limit of CMOS with the techniques above being taken to their limits and the device physics becoming ever more theoretical. Silicon nanowires – horizontal and vertical – quantum well transistors, junctionless transistors, heterojunctions and other tunnelling devices, memristors and various carbon structures on silicon are all being researched and these processes may need to be built on wafers different to the ones currently being used.

Aside from the processing issues at 8nm and below, quantum effects become a major factor requiring changes across the whole IC design methodology. At these node dimensions transistors are essentially free but unreliable. All of these approaches require very different design rules to those currently in place and whoever masters these first will see a huge financial and competitive advantage. At the same time interconnect becomes relatively more expensive and so design methodologies will have to focus on logic error correction techniques combined with reducing the number of interconnections, for example by the use of Network on Chip techniques.

Moving into the second half of the 2020s, Intel has suggested silicon based structures that operate all the way down to 3nm will still dominate. However many believe that by this time the active elements will tend towards a dominance of carbon based structures – graphene, diamond, benzene ring and the other possibilities being researched – but it is currently envisaged that these will be built on some form of silicon wafer for some years to come. However this wafer will require considerable pre-processing, adding to its cost and value.

European universities are amongst the world leaders in graphene with researchers at Manchester University already winning the Noble Prize for its discovery. Both the EU and US are funding advanced research in this material and we can expect the first graphene on silicon wafers to appear over the next few years.

At first graphene imposed a limit on the wafer diameter size as there was no way of creating large sheets of graphene and bonding them to a silicon wafer. However it has recently been demonstrated that a silicon carbide layer can be converted to graphene by the use of a laser, a process which can be performed during IC processing or directly after wafer slicing, removing the restriction of wafer size diameter. By the time graphene reaches full production, it may even be possible to deposit it directly onto a bulk or SOI wafer, possibly using a derivative of Soitec's Smart-cut method.

We expect that all of the other problems, such as creating a band-gap in graphene and reducing the 'off' current to an acceptably small level, will have also been solved by then and that carbon based devices will eventually supplant silicon as the prime semiconductor mterial.

That said, quite how graphene wafers will eventually be processed is not yet known but it seems reasonable to assume it will be based on techniques and equipment developed for normal silicon wafers, with the first graphene devices entering volume production in about 10 to 15 years time on 450mm substrates.

6.4. Semiconductor Processing

Producing ever decreasing geometry sizes is not an easy task. The key process technology to achieve that is lithography whereby features from a mask set are exposed onto the wafer for etching and deposition of other materials. Traditionally smaller geometries have been achieved by shortening the wavelength of the laser used to expose the resist. However the move to the next step and potentially very expensive Extreme Ultraviolet lasers (EUV), was avoided for many years first by the use of immersion lithography and its further extension thanks to new but more expensive double or multiple patterning techniques.

Despite the difficulties encountered in its development, the additional cost of multi-patterning makes EUV a mandatory step to enable scaling down to 5nm as recently confirmed by Applied Materials' CEO Mike Splinter during a presentation at SEMI's US Industry Strategy Symposium in January 2012. It is thus fortunate for the industry, and Europe in particular considering the leadership of ASML in this field, that EUV lithography is now becoming viable. The first prototype machines have already been delivered with pilot production machines due for delivery next year and full production machines a few years after that.

Quite fortuitously this corresponds with the transition to 450mm wafers so, whilst the early machines will have 300mm tables, we expect the full production EUV machines to focus primarily on 450mm wafer processing.

The position of leading-edge IC makers on the insertion of EUV in their manufacturing strategy varies depending on their technological portfolio and market position. NAND flash memory makers are extending the life of 193nm immersion lithography down to 2xnm and 1xnm nodes whilst DRAM vendors are eager to use EUV as early as possible for the critical layers of their next device technology. Intel plans to insert EUV at the 10nm node and rely on multi-patterning and immersion lithography down to the 14nm node. TSMC plans to extend 193nm immersion down to the 20nm node and is evaluating EUV for critical layers at 14nm node whilst GlobalFoundries plans to use both EUV and double-patterning at 20nm.

Whatever the product category or chip manufacturer, EUV will however coexist with other lithography technologies over a period of time since it will first be required only for critical layers of the device while upper layers will still rely on conventional immersion tools.

Finally, it should be noted here that additional lithography technologies are also researched such as mask-less electron beam (e-beam) lithography and nano-imprint, both of which will be used to provide prototyping capabilities and enable advanced process development to proceed in advanced research facilities. The European firm MAPPER is the current world leader in e-beam lithography.

6.5. Other Advances In IC Design

Over the history of the semiconductor industry, most focus has always been on the newest and most dense nodes. This is understandable but does not mean ongoing advances are not being researched and achieved in larger nodes. For example power devices use much larger feature sizes than the state of the art but are in many ways just as advanced with the focus being on removing heat from the die to achieve a greater power handling density. Other products such as MEMS are also fabricated in larger geometries. Of course both of these areas happen to be areas of expertise in Europe.

One area which raises a lot of discussion is analogue circuit design. Traditionally analogue feature sizes follow those of digital but lag two to three generations. This meant it was still usually better to put the analogue features on a digital IC but with larger feature sizes.

The smaller voltages used for the latest logic nodes, combined with the option of 3D integration, opens the possibility for the analogue functions of a SoC to be made on a separate die using an older capability fab and then mounted on top of the main digital IC.

Whilst we believe this will happen it should not be assumed that state-of-the-art analogue will not carry on following the digital feature size curve. Indeed the first analogue cell libraries using Intel's 22nm TriGate transistors are already being designed which may move analogue nearer to the digital feature sizes than has been typical in the past.

It is thus essential that European design expertise in analogue circuits is not used as a reason for not investing in leading edge nodes within Europe as without access to the latest nodes these skills will quickly become out of date.

Although 450mm and advance-state-of-the-art processing have become de-facto synonymous, we do not believe that the future wafer size transition needs to be restricted to leading edge nodes as history tends to indicate. Instead we propose that processing non-leading edge geometries first would actually de-risk the 450mm transition by providing a platform to run proven technologies with a well proven market. Indeed we believe such a European-based, non-state-of-the-art node fab could be up and running long before a fab running leading edge processes. This would provide an advanced manufacturing platform for Europe's MtM-based technologies at a far lower cost than 200mm and 300mm fabs and establish Europe as the clear leader in this field.

It must be emphasised though that, whilst it is an area of European expertise and does promote an active semiconductor industry in Europe, a strong Moore than Moore capability does not help Europe address the needs of the post-CMOS era. It is thus essential that access to these advanced technologies is guaranteed for European companies, large or small, otherwise the consequences for Europe will be irreversible long-term industry decline.

A European-based, non-state-of-the-art 450mm wafer fab would provide the necessary conditions to allow Europe to consolidate its current MtM global leadership on a lower cost-base structure and provide a gateway to catch up on advanced CMOS logic processing ensuring its longer-term leadership as well.

This option is discussed in more detail later on in the Report (see Chapter 17).

6.6. 3D Integration

Long before 450mm wafers are in production, many semiconductor products will be using multi-die processing whereby fully processed and tested silicon die are mounted on top of each other at the packaging stage. This method is used to provide more active silicon area inside a given size of package and there are two general approaches to such 3D integration.

The first is termed 2.5D where active dies are flip mounted side by side onto a larger silicon interposer which just provides interconnections between the die and is generally fabricated in a 65nm node metal process. The main use of this technique is in FGPAs and network processors where large numbers of interconnections are required and stacking active die on top of each other could cause overheating.

The alternative is the 3D stacked die construction whereby the bottom die is an active die and other similar or smaller die are mounted on top. Probably the most well know example of this technique are the A series of processors in the Apple iPhone and iPads which mount DRAM die on top of an SoC providing processing and other functions.

A new technology just appearing involves stacking the die several layers high and routing directly through the die using what are known as Through Silicon Vias (TSVs). This technology is still in its infancy but offers significantly higher packaging densities. It also reduces system power consumption as the line drivers now only have to drive the millimetre or less interconnect between the die up and down in the stack, rather by the longer distances required by other techniques.

The increased wafer thickness of 450mm wafers will be an issue here and back-grinding of the wafer may be necessary. This is beginning to get significant coverage with lots of questions being asked, for example the impact of increased back-grinding on device yield and life.

However 3D integration will happen no matter what the status of 450mm processing technology is. It is essential though that it is not be seen as an alternative to 450mm processing for achieving greater density and keeping to Moore's Law on a per-package basis. Even ignoring whether advanced nodes are available on 300mm, as we explained in previous section, dies sourced from 450mm wafers will be cheaper than those from 300mm wafers no mater what the process node and so it is essential 450mm processing is available to provide die at competitive prices for European companies integrating dies in this manner.

6.7. Semiconductor Process Technology Conclusions

The combination of a complex and unclear process technology roadmap, design methodology changes and the move to 450mm coupled with the uncertainty of new wafer patterning techniques such as EUV, e-beam, etc, combine to represent the biggest challenge the semiconductor industry has ever faced and will undoubtedly require further considerable public support for the appropriate research and industry co-operations.

Thankfully Europe's Industrial policy is currently benefiting from a renewed interest from policy makers, with a strong emphasis being given to the advanced manufacturing activities in selected Key Enabling Technologies (including semiconductor technologies) that are necessary to master innovation and meet future society needs, especially the ageing population, security and environment issues.

7. 450mm Fab Sizing & Loading Models

This chapter considers the details of 450mm processing and concentrate in particular on one key consideration which is to explore the optimum fab size for each type of fab in order to establish which type(s) is (are) best for Europe.

7.1. Research Labs

Firstly we consider the small research labs. Most of the major players have their own research labs but it is obvious that many are becoming technology followers. The significant labs in world terms are, in alphabetical order listed below, although not all of these are at the same level of competence, with many just focusing on specific technology niches.

- CNSE/Sematech
- Fraunhofer
- Fujitsu
- Hynix
- IBM
- IMEC
- Intel
- ITRI
- Leti
- Micron
- Renesas
- Samsung
- Toshiba
- TSMC
- UMC

Of these, we expect only CNSE, IMEC, Intel (Oregon), Samsung and TSMC to be able to process 450mm R&D wafers during this decade.

It is to Europe's strength that IMEC is at the top of this list in terms of overall advance global semiconductor research lab competence.

Intel is of course the dominant world semiconductor manufacturer and the most technically competent, with solutions and a back-up plan lined up all the way up to at least 3nm, the technical details of which will be discussed later in this Report. They supplement their own research by funding research at a number of other universities worldwide and also fund directed projects at several research establishments, including IMEC in Europe.

Thanks to the successful policy of funded research, Europe is a great generator of basic technologies and world-class research labs but this strong research capability has not recently been aggressively followed through by Europe's indigenous semiconductor firms, allowing the USA, and more specifically the Albany cluster which combines both equipment and process R&D, to steal the advantage at 450mm.

TSMC is rather different to the others in that part of their front-end research is performed at IMEC but even they have been obliged to join the Albany cluster to transfer this R&D into a production process. They also have a strong tendency to evolving Intel's advances towards their own specific needs.

7.2. First 450mm Production Fabs

At the other end of the scale, all three early 450mm adopters produce ICs in huge unit volumes. As such they can readily justify and afford to build large fabs, with Intel and TSMC both planning to leverage work carried out at Albany and IMEC. Both will first build a pilot line that will be readily scalable up to mass production volumes, for Intel at D1X in Oregon and for TSMC inside one module at Fab 12 in Hsinchu.

TSMC appears to want to begin building its 450mm pilot line very early, in the 2013 period utilising 20nm technology whilst, according to P. Gargini's statement during the last EEMI450 General Assembly on April 13th 2011, Intel is talking about 2015 with a development phase based on processes between 20nm and 30nm but compatible with the 11/10nm node. We believe there to be a strong element of PR in the TSMC dates (as confirmed by IMEC during the 1st Focus Group meeting on March 28th 2011) as the 450mm equipment will not be ready for production by this date.

Intel's dates appear to be much more realistic given that their 11/10nm technology is scheduled to enter production during 2015. It also confirms our likely 450mm roll out scenario, Figure 5 (see §5.5.3) of running in the 450mm production line on a relatively mature (32nm) process, rapidly moving to 22nm for the early test wafer and demo tools, moving rapidly to 16nm for the first generation production tools (i.e. both at their respective 'n-1' time line), flipping to 11/10nm as soon as there is confidence that the line is robust.

It further underscores our view that the first generation 450mm production equipment will be 11/10nm ready, thereby allowing a more carefully co-ordinated, and instantaneous, switch. Thus, whilst at first sight this might give the appearance that 450mm was being introduced behind the 300mm node curve, the reality is quite the opposite. Once the 450mm production bugs are ironed out, 450nm will overtake and replace 300mm at n+1 and all future nodes.

Samsung has yet to make any public announcements on its transition plans but in practice we expect all three companies to be very similar in timescales, all using initial work carried out in Albany which offers a unique combination mixing equipment and semiconductor process R&D under the same umbrella. We expect Albany to be operating a full 450mm pilot line in the 2014-15 timeframe, capable of running possibly up to 3k 450mm wafer starts per month, i.e. about 100 wafers or 4 batches per day, equivalent to 15k 200mm equivalent wafer starts per month. It is unlikely however to ever achieve this capacity as there will be regular breaks in processing whilst problems are ironed out.

The transition to 450mm also represents a major step forward in automation and we expect all elements of this will be included in Albany and all other pilot lines so that this aspect is also fully debugged before full volume production starts.

At some point before the pilot lines reach full capacity, the decision will be taken to begin equipping full production fabs. We expect Intel to expand D1X in Oregon and then fully equip Chandler in Arizona, whilst TSMC will equip their new Fab 15 at Taichung. Assuming

all problems have been ironed out in the pilot lines, the first full production line will typically take at least three to six months lead time from order to delivery of the initial equipment set.

This is followed by six months to hook up, qualify technology/products and get production ready followed by a three months first production cycle and finally a further 6-18 months to ramp to full production during which time additional equipment is ordered and hooked up until the fab is fully equipped. Subsequent expansions can reduce this cycle time based on past experience but there is an element of risk in this and the time gains are usually less than expected.

Both locations are clearly capable of being expanded to full scale production of at least 50k 450mm wafer starts per month (250k 200mm equivalents). Both will expand the fab modules to full production in steps, typically of around 10k-15k wafer start chunks, and we would expect both fabs to expand to their full capacity in most probably three phases.

Intel's D1X fab is being built to be 450mm capable, notably in areas such as clean-room floor height, cooling, power distribution and suchlike, but will be initially installed as a 300mm line in order that the fab will productive from the start. The 300mm equipment will thus need to be removed at some time during the 450mm build out.

Whilst Samsung has not made any public announcements yet, we can safely assume it will be of similar magnitude to the above.

7.3. 450mm Fab Sizing

The interview process examined various issues as deeply as possible at a generic, non-company confidential/specific detailed level. The key findings are outlined below.

Research fabs aside, such as at IMEC in Belgium, there is a wide diversity of 300mm fab sizes, ranging from STMicroelectronics' facility in Crolles-2 to TSMC's Fab 12 and Fab 14 which are roughly ten times larger. We do not expect to see such a wide disparity at 450mm.

The first issue that will change with 450mm when compared with 300mm is that of automation. For 450mm a FOUP (Front Opening Universal Pod) or FOSB (Front Opening Shipping Box) loaded with 25 wafers will weigh over 35kg and so manual lifting and insertion becomes impossible. Thus the fab needs to be fully automated from day one.

The second issue is that although the oxidise/resist application/photolithography/etch/deposit cycle is repeated many times for a wafer, it is not possible to use the same machines throughout the process. For example once copper has been deposited on a wafer then that wafer can never be allowed to enter a machine earlier in the process as the copper will pollute the machine and reduce yield considerably. For similar reasons most dopants and gases are applied in dedicated equipment and with the number of these increasing, the quantity of equipment does likewise. Although not directly related to the wafer size, this issue will directly influence advanced 450mm wafer fab sizing.

For efficiency reasons, a fab should seek to have all equipment operating all of the time and so the appropriate number of the more often used equipment needs to be installed so as to balance the line.

At the beginning of this project our expectation was that the optimal 450mm production fab module size would be around 20k 450mm wafer starts per month and that this module size would be replicated to achieve greater fab output, as was the case with 300mm fabs. As the research progressed, however, it soon became clear that both the Intel and TSMC 450mm fabs would be built with an end goal of around 50k wafer starts per month, with the initial pilot line built as the first phase of the production fab. Both pilot lines would be the minimum module size commensurate with a reasonably well-balanced line with this line expanded using a 'Copy Exactly' approach.

7.4. 450mm Fab Questions

Many questions were asked on fab sizing, pricing and related topics during our interviews with the industry. The full list of questions is given in Appendix 2. The often rather vague answers are summarised below:

- Production fab cost will be 'around US$10 billion'. Nobody gave a significantly different number and we provide later on in this Report some cost estimates and extrapolations that tend to confirm this number (see Chapter 17)
- Fab modules will be 60 percent larger than existing ones, i.e. an MPU clean room will cover a surface of 50k m^2
- A primary issue in setting this is the size and weight of the EUV machines
- 450mm wafers themselves do not increase the fab size significantly. 300mm EUV machines are just as large as 450mm ones
- According to several sources, a European 450mm pilot facility could cost around US$1.5 billion
- The main advocates of a European 450mm fab were the equipment manufacturers for whom just a pilot line is satisfactory
- The European IDM and fabless semiconductor companies expressed far less interest in a full 450mm fab and indeed some were hostile to the concept arguing Europe should invest in other 'more important' things
- Support equipment costs (gas supplies, water and power distribution) are not really that dependent on fab capacity at all. The larger the fab the lower these costs will be apportioned to each wafer
- The industry is aiming for a circa 30 percent die cost gain, i.e. roughly the same as the 200/300mm transition. It is accepted this will not be immediate though
- The main technological or strategic advantages from possessing 450mm technology will only become apparent once a node is reached where 300mm development has ceased

- Pods will still be of 25 wafers and usually expected to be full. Thus the number of die for a run will increase by 2.25 times. There will still be 300mm fabs to handle smaller quantities for several more generations

7.5. Advanced Semiconductor Production In Europe

In the past Europe has taken two different approaches to moving advanced semiconductor R&D to production.

Infineon (then Siemens) in partnership with Motorola (now called Freescale) drove the 300mm transition with their Semiconductor 300 joint venture in Dresden in 1999. This was capable of producing 3.5k 300mm wafer starts per month. Once the pilot line was proven, Infineon embarked on an aggressive build out and expansion of the Dresden site, during which time the plant was expanded in several stages up to 35k wafer start per month, whilst Freescale opted to partner with STMicroelectonics and NXP in the smaller scale Crolles-2 lab fab initiative.

The Dresden operation was subsequently spun out from Infineon and renamed Qimonda. It was maintained at the state-of-the-art until it hit financial problems and was closed due to the collapse in the price of DRAMs at the latter part of the last decade.

Crolles-2 in contrast promoted the use of a much smaller and jointly owned lab-fab to develop new processes and debug new equipment with the intention of then transferring this knowledge to much larger fabs at a later date. However no large scale fabs were ever produced by any of the partners from the lab fab experience.

7.6. European 450mm Fab Sizing – Lab-Fab

It has already been determined that the majority of 450mm equipment debug will occur at the 450mm wafer development centre at the CNSE/Sematech centre in Albany, NY. Although Albany will not produce any significant volume of finished wafers, its larger scale compared with previous transitions will ensure all items are fab-ready ensuring there is less of a risk to roll-out of a large scale pilot fab at Intel D1X and elsewhere.

A further offsetting factor is that 450mm fabs will be far more automated than 300mm ones, meaning full scale automation will be mandatory at 450mm whatever the capacity of the fab. It will not be possible to optimise these automated sequences in anything smaller than a large pilot line, or indeed gain the full advantages of that automation in anything less than a full scale fab. It might even be automation that determines the minimum feasible lab fab size.

If the 450mm transition follows the routing outlined above, the risk in moving directly from pilot line to a full-scale fab is quite low. Conversely the risk of not moving is actually much higher given (a) the cost advantage a large scale fab would have over a lab fab and (b) the fact that the minimum size lab fab is still some considerable size.

7.7. 450mm Fab Models – Conclusions

Arguments presented above tend to indicate that if Europe is to enter the 450mm semiconductor manufacturing arena it needs to be on a scale to match major world players.

As of today ST, Infineon and NXP, due to their last 10 years strategy of outsourcing advanced 300mm processing, would appear unlikely candidates for early 450 mm adoption, indeed they are on record as stating they do not need 450mm until at least 2020, if at all.

This leaves Intel in Ireland and GlobalFoundries in Dresden as the only two European-based firms expressing any interest in 450mm production, with the outside possibility to encourage (entice) currently non-European based firms (e.g. Samsung and TSMC) as well.

Given the March 11 earthquake and tsunami in Japan and the fact all of TSMC's advanced foundry capacity lies on the same fault line in Taiwan, albeit in two separate locations, given the right incentives, 450mm might represent an ideal dislocation point for TSMC to build their first foreign state-of-the-art facility, uniquely leveraging their relationship with IMEC and Europe's strong IP and equipment skills in 450mm processing. There is a far less compelling argument regarding Samsung's position.

8. Industry Impact Of 450mm Processing

8.1. Effect Of 450mm On Existing 300mm & 200mm Manufacturing Infrastructures

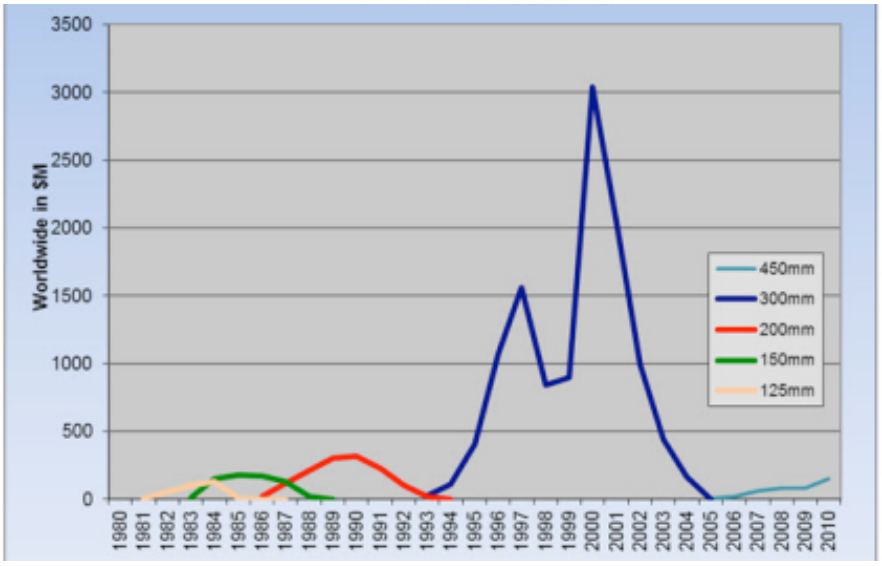
It is likely that the transition to 450mm processing will have a major effect on smaller diameter wafer fab processing infrastructures as already demonstrated in past transitions. At the beginning of this project, two scenarios were possible with rather different consequences on the semiconductor supply chain, namely:

Scenario 1: the 450mm wafer size transition could follow a similar pattern to the 200mm to 300mm transition making it most likely that future processing technologies will only be developed for 450mm.

Scenario 2: 450mm transition would remain focused on just those products that had large production volumes, leading to a situation whereby node development was sustainable on both 300 and 450mm platforms, albeit with the associated 300mm tools slightly delayed.

At the 200/300mm transition, the transition followed Scenario 1, with future node technology developments effectively ceasing on 200mm equipment, Figure 7, with only minimal improvements made thereafter, forcing all future advanced technologies to the 300mm platform. This had the effect of spawning the IDM 'Fab-Lite' concept, with the large logic foundries, especially TSMC, the market beneficiaries.

Figure 7 – Equipment Industry Spending To Develop New Wafer Size Platforms



Source VLSI Research (2011)

It soon became clear during the interview process that there was little enthusiasm from the equipment manufacturers for continuing with 300mm developments in parallel due to the additional R&D costs and limited 300mm market size and there is now an industry consensus that, starting with 5nm (possibly even as early as 8nm), advanced technologies and post-CMOS processes will only be available on a 450mm platform.

Whilst this does not imply that existing 300mm fabs will be rendered obsolete and it is possible that there will still be a degree of cross-fertilisation from 450mm technologies into the current 300mm infrastructure so as to improve productivity, it will significantly restrict their target markets to more specialist areas such as analogue, smart power, specialty products and MtM activities.

It is thus likely that once 450mm fabs are being opened in volume, the fairly large number of 300mm fabs worldwide will eventually be competing for the same business which might trigger over-crowding, over-capacity and some fab closures. However as the 200mm fabs have shown, there will always be a market for devices produced on smaller wafer sizes in older technologies, whilst specialist technologies such as analogue, sensors and MEMs can be expected to migrate from these to the 300mm wafer size in due course.

This chain reaction will however put the 200mm manufacturing infrastructure competitiveness under strong pressure due to both limited technology improvement and Cap Ex extension capabilities with many more fab closures to be expected (similarly to what happened to 150mm fabs following the 300mm transition). Such an impact is expected to materialize within the next 10 years and once 450mm fabs will be producing in volume.

From a practical point of view, despite the ongoing need for greater integration, the sheer scale and cost of 450mm wafer processing is likely to make on-chip fabrication of analogue and sensor functions uneconomic, which will have the effect of driving a parallel transition to multi-die System in Package (SiP) products so as to integrate analogue and sensor functions into the same package.

It is thus quite likely that specialist development of 300mm processing equipment will still continue so as to enable these functions necessary for the full system to advance as required. One area where this could be critical is Through Silicon Via (TSV) processing, an area that is expected to grow rapidly in order to build systems combining die from 450mm and 300mm fabs. Current 300mm fabs will need some upgrading to be able to achieve this effectively but the equipment for this is already in development.

Finally, one worry we heard from IC users is that the transition to a 450mm only future means that low and even some medium-volume products would either be excluded from future technology nodes or driven into a de facto TSMC 450mm foundry SoC logic monopoly. However this is really little different to the current situation on 300mm at the advanced nodes whereby a few companies produce products that can be used in a variety of applications, often with major parts of the die powered down.

One point we do wish to emphasise here is that there are no technical barriers preventing more mature technologies from being manufactured on 450mm wafers, provided the volumes are there, indeed this is an integral part of the 450mm roll out. Furthermore, such a move is inevitable once the first 450mm depreciated fabs and equipment start to be available in 10 to 15 years from now, quite similarly to current events with analogue and power products moving from 200mm to 300mm.

The point we wish to emphasise here is that mature node 450mm production could also happen much sooner, by strategic decision rather than natural default, with the substantiating arguments developed later on in this Report (see Chapter 17).

It is our belief that a European-based 450mm fab focused on MtM products should be built in parallel with the early-adopter's 450mm MM fabs. Not only would this be a natural fit across the full spectrum of Europe's current semiconductor industry base, it would also help accelerate the overall 450mm transition.

8.2. Upgrade Of Existing 300mm Fabs & Tools

When the 450mm fabs will be deployed, the remaining worldwide 200mm fabs in activities will be reduced in number and focused on low costs operations with extremely limited opportunities to receive Cap Ex for potential upgrades. Potential cross-fertilization from 450mm development to below wafer size will thus essentially be limited to 300mm manufacturing infrastructure and tools.

From a fab building perspective, a key issue is that many 300mm fabs are too small to accommodate the new equipment required to convert to 450mm wafers. It is not just the floor area, but ceiling height and floor strength. This will certainly be an issue for EUV lithography, probably fab automation as well. If new greenfield production sites therefore had to be built, as would be the case for Crolles, the overall investment dynamics might not make economic sense (see Chapter 7.2). Better perhaps to consider building a full scale 450mm fab in conjunction with a partner or as a chip-makers consortium, similar in concept to those successfully used in the aircraft industry.

The most recent 300mm fabs have been constructed to accommodate the ceiling height, especially the under floor height requirement for the 450mm wafer processing equipment but we believe the only fab in Europe meeting this need is the new 300mm Global Foundries building in Dresden. This means that any new 450mm fab would need to be Greenfield with the cost of a new shell and facilities added in.

Another key issue that was discussed at length is the use of EUV lithography. Although there are still issues with the power output of the lasers, it now seems likely that EUV will play an essential role at the 11/10nm node, the current node pencilled in as the crossover point between 300mm and 450mm wafer processing, but that early production EUV equipment will be 300mm only but still large enough to exclude any 300mm fab that was not 450mm-ready.

Alternative techniques such as nano-imprint and e-beam are also being investigated and indeed nano-imprint will be used for early wafers made at CNSE Albany. TSMC had hoped that the use of e-beam would allow it to get an early start on 450mm wafers but this appears to have subsided in recent months, although the company remains involved and active in the IMAGINE European programme on Mask-Less Lithography.

From a fab automation perspective, up until the Intel and TSMC 450mm announcements, significant discussion was taking place on next generation automation for 300mm fabs. It is now quite clear that these discussions will be shelved with activity now focused on 450mm wafer handling. We do not believe much of this work will be retrofitted to 300mm fabs but some improvements will trickle down on both hardware and software development.

From an equipment & material perspective, 450mm development will drive incremental innovations in wafer handling & manufacturing, process tools and metrology that could be retrofitted to 300mm to improve the competitiveness of the existing manufacturing installed base. Such areas of potential cross-fertilization are summarised in Figure 8.

Figure 8 – Possible Cross-Fertilization Areas From 450mm To 300mm

Technical domain	Cross-fertilization opportunity from 450mm to 300mm
Wafer handling & manufacturing	450 might lead to develop small volume device batch size, something that is not completely solved so far on 300mm
	Manufacturing Tactics to maximize the equipment up time
	Non-contact wafer handling (mandatory in 450mm process)
	Inverted linear motor system for robot handling wafer
	450 litho tools will have to be equipped with lighter stage ▪ Lighter weight wafer chuck ▪ Litho Scanning speed must be improved for 450
	Efficient power dissipation chuck
	Efficient thermal dissipation on chamber
	Wafer edge control of the wafers will have to go to another level of accuracy
	Gas purity & delivery technics in chambers for better wafer in wafer (WIW) uniformity of deposition will have to be developed
	Multizone control across wafers will be mandatory for 450
	Wafer transfer system on tools developed in 450
Metrology/Process control innovation	Technical performances for Metrology tool/analytical tools developed in 450
	Gases purity/gas logistic systems developed for thin film solar & 450
	Improved advanced process control (A.P.C.)
	Thermal control of heat distribution on wafer
Materials/Equipment	New ceramics
	New CMP Techniques/CMP Materials
	New R.F. High density PLASMA generators from Manufacturing experience in Solar thin film
	New PLASMA etch and plasma distribution for sensitive architecture
	New vacuum pumps currently developed for thin film solar
Process Step	New process step developed for 450, when they will be independent from 450 tools, will be directly deployed to 300 current process steps

The overall impact of 450mm to 300mm cross-fertilization essentially relies on tool and material suppliers' strategies. Since we expect those heavily investing on new 450mm platform will first try to secure and consolidate their 450mm business rather than maintaining in parallel a competing state-of-the-art 300mm platform, we do not expect to see a huge spin-off of 450mm development advances onto 300mm tools.

8.3. Summary & Conclusions

The 450mm transition will impact the existing SC manufacturing infrastructure competitiveness to different degrees and timescales.

200mm fabs will experience the earliest and strongest impact since 450mm fabs will generate 300mm spare capacities that will seek to penetrate 200mm markets quite similarly

to what happened to 150mm fabs following the transition of advanced CMOS technologies to 300mm.

300mm speciality development will be stimulated but scaling and 450mm upgrade capabilities will be limited forcing players willing to maintain internal production of state-of-the-art technologies to consider new Greenfield investment or partnerships.

Cross-fertilization from 450mm to 300mm will happen but is likely to remain limited however for the following reasons:

- The degree of cross-fertilization will mostly depend on tools suppliers' willingness to transfer 450mm innovation onto 300mm platforms. This is unlikely to happen at least in the short term since most players will rather try to secure and consolidate their 450mm business first

- 300mm available Cap Ex will be fairly limited once 450mm will be on production since the only players investing in 300mm are precisely those, with very few exceptions, that will concentrate on 450mm

Europe has missed the 300mm transition and the European SC manufacturing base is now mostly composed of 200mm fabs with only few 300mm sites with Intel (Dublin), Global Foundries (Dresden), STMicroelectronics (Crolles) and more recently Infineon (on-going project in Dresden).

Europe is therefore highly exposed to the medium and long-term impact of the 450mm transition. One could say that a European strategy would consist in consolidating and expanding the existing 300mm base as it is being advocated by some European IDMs, however we doubt this 300mm investment strategy would bring any benefit to Europe since it will not make any economic sense to invest in new European 300mm capacities when depreciated 300mm fabs will be available in Asia following the 450mm transition.

We do however believe that any EU 450mm vision for advance manufacturing must embrace both 300mm and 450mm and their combined innovation opportunities into a single long-term plan.

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9. Impact On Equipment & Materials Technologies

Europe has many companies operating in the semiconductor equipment area including vacuum, UV/EUV/X-ray sources, optics, handling, CVD, PVD, gas network and abatement systems, several of them world-leading. It is strategically important that their leadership is maintained.

Conversely Europe has less interest in wafer testing, scribing and packaging although equipment should be able to support 450mm wafers with the same automation level that is planned for the Front End fabs.

By whatever measurement criteria, the disruptive impact on the equipment industry and technology of both the 450mm transition and the move to smaller node structures will be something more profound than it has experienced previously.

The move to ever smaller device structures will also require an expansion in the range of materials used. Some of these can no longer be considered in isolation for the 450mm substrate size change.

9.1. Lithography

Advances in process nodes require big steps in lithography techniques, with 32/28nm using second generation of immersion lithography, 22/20nm Source Mask Optimization (SMO) together with third generation immersion lithography, whilst 16/14nm will require fourth generation immersion lithography, SMO and double patterning.

Source Mask Optimization (SMO) is a method of changing the light source to work around mask limits. Masks currently use diffractive optical elements (DOE) to make patterns smaller than the light wavelength used to draw them. SMO adds a pixelated light source to enhance mask creation. Europe's ASML and Zeiss are both working in this area.

The point at which EUV will be introduced is still undecided. Many believe it will be necessary for some, though not all steps, of a 16/14nm process, whilst others believe even 11/10nm may use double or triple patterning. Whatever the chosen solution, ASML is the acknowledged world leader here.

Another approach for very advanced nodes is e-beam lithography and this may be introduced for some applications for sub-14nm nodes. Europe also has a leadership in this segment with MAPPER.

9.2. Deposition

ASMI and Aixtron are the world's leading players in the field of depositing various substances onto the base wafer. The larger surface area and smaller details for advanced nodes will make uniformity ever more important and whoever best meets this challenge will gain a significant commercial advantage.

9.3. CMP

The CMP process changes needed for 450mm raise several questions at the substrate manufacturing level and the different CMP steps of the wafer flattening process. The key question here is whether it will be possible to obtain the required flatness, thickness control and cost over the significantly increased wafer diameter.

9.4. Wafer Handling

The transition to 450mm is regarded as the next big step in wafer fab automation, with FOUP specification and standards already in discussion within ISMI. Europe's wafer handling, companies, such as RECIF and others, will need to meet this challenge.

9.5. Metrology

450mm metrology needs are coming from the sum of the wafer size effect and of the advanced technology nodes expected to be processed.

Due to the fab organization already largely explained, it is clear that all the metrology equipment will have to be fully automated and connected to the CAM (Computer Aided Manufacturing) and handling systems, this approach is new for a lot of equipment and they will have to be developed accordingly.

Those metrology tools will be in continuous closed loops with process tools. All manufacturing tools parameters will be driven by measurements done on metrology tools, this being monitored and controlled under a new generation of advanced process control systems (APC).

A new table will have to be developed due to the wafer size and the throughput objectives (time factor x2.25 if serial), with efficient coordinate system (XY is already a serious difficulty at 300mm).

Due to advanced nodes requirement, more performing equipment for surface/film analysis on vertical surface (1nm to 10nm), 3D characterization from atomic to wafer level, all lithography metrology and interconnect metrology are to be developed, together with more efficient correlation tools.

9.6. Cross-Fertilisation With PV & LCD Processing

Given that the Photo-Voltaic (PV) and LCD industries have already mastered handling and processing very large substrates, it seems possible that there might be a degree of cross fertilisation and potentially significant development cost and time savings by working with the current PV and LCD equipment suppliers, especially in the areas of:

- Large size/volume deposition chambers

- Large size/volume CVD clusters
- Large size vacuum pumps
- Techniques to monitor temperature gradient across large dimension substrates
- Large size substrate handling
- Manufacturing tool loading/unloading processes
- PV thin film tools
- Specialty gases & bulk gases
- Safety system around gases leaks detection

9.7. Wafer Production

Companies working on wafer development note that producing 450mm substrates with the extreme levels of purity and smoothness demanded is not going to be easy. With the fast growing solar market as an alternative focus, we can expect some suppliers to concentrate their research and production efforts on lower-cost solar-grade production technology. There is also an issue of whether the industry will need bulk and/or SOI wafers, or even, in the longer term, even more complex wafers.

Pulling the 450mm ingots from the larger crucibles of melt would leave a lot of polysilicon waste unless the ingots are grown long enough to use most of it up. SUMCO Corporation has calculated that a 450mm ingot will need to be about one tonne in size, approximately three times the weight of a 300mm crystal, in order to keep the material waste to about the same level as with 300mm wafers. Fortunately this is still within the 1250kg tensile strength limit.

The 3m length of the ingot will also be much longer than current 2.4m long 300mm production, necessitating not only larger crystal pulling equipment but possibly also a new support system to supplement the usual 3mm neck used to start the growth of the pure single-crystal ingot and from which the entire ingot then hangs whilst it is pulled from the melt.

Another issue is that the time needed to heat up and cool down this larger mass of material will be two to four times longer than that for 300mm wafers, which in turn means a lower production throughput and a higher density of defects. These nearly half-meter wide wafers are also going to have to be thicker once sliced in order to maintain the same stability against bowing and sagging as for current 300mm wafers.

Issues and concerns aside, global 450mm wafer specification and standards are already well advanced within the SEMI organisation.

9.8. Gases

We have not identified any special gas needs directly related to 450mm wafer processing. It is however likely that the gas handling system and corresponding worldwide logistics will be inspired by what has been developed for the Flat Panel Display and Solar Photovoltaic industries.

9.9. Dopants

As with gases, the dopants needed do not depend on 450mm wafer processing but will undergo significant changes around the time of 450mm wafer introduction due to the finer device geometry requirements. Common dopants such as Boron, Arsenic and Phosphorus have already been supplemented with a selection of other elements, with the following possibly needed at the 450mm transition, depending on the node:

- Group 2A: Strontium
- Group 3A: Gallium, Indium and possibly Thallium
- Group 4A: Carbon and Germanium
- Group 5A: Antimony
- Transition Elements: Hafnium, Molybdenum, Ruthenium and Tantalum

Again, although independent of wafer size per se, dopant waste recycling will add another layer of complexity and the 450mm equipment will need to be designed to eliminate the waste of the rare earth material that will be used in the process. This is especially important given the fact that most of today's dopant usage leaves the fab as waste rather than as part of the processed wafers.

9.10. Low-k Materials

As with dopants, the use of Low-k materials is not directly dependent on 450mm wafer processing but have been identified by the ITRS as potential roadblocks on its roadmap. However over the course of this project we have become aware of European research in this area potentially solving most of the problems once it becomes commercially available.

9.11. Slurries

The big issue here is whether slurry cost will become prohibitive due the increase in pad area. The new requirements on slurries was discussed during Task 2 interviews, along with CMP issues in 9.3 above.

9.12. Masks

Masks should also be independent of wafer size other than the possible use of EUV lithography for some operations. This position was confirmed during the Task 2 interviews.

9.13. Security Of Supply

One issue frequently mentioned is the industry's current over-dependence on often one or two dominant sources for materials supply, for example the rare earth class of materials for which China currently supplies over 98 percent of the market. Increased demand has seen the price of these increase and even supplies of common metals, such as copper and aluminium, have seen price increases recently due to strong world demand.

The 11 March 2011 earthquake and tsunami in Japan has also exposed how dependent the semiconductor market is for 300mm wafers, plastics, and other crucial materials on just a few quasi-monopolist suppliers, with devastating effects on the downstream value chain.

EU policy could play a crucial role here, especially with regards to recycling policies, given that the dominant proportion of all materials used by a wafer fab in the manufacturing cycle, other than the silicon wafer itself, end up as waste.

Europe already has the strongest 'green' credentials in the world and this may be a new area that Europe can dominate.

9.14. Conclusions

Europe's research establishments and equipment and materials firms are still at the global technology state-of-the-art and forefront of the 450mm transition. Programmes such as ENIAC and CATRENE currently support these leadership positions thanks to dedicated 450mm projects such as CATRENE's NGC/SOI450 or ENIAC's EEMI450 but also a variety of technology projects whose results will be exploited at 450mm (e.g. LENS, MERCURE, REFINED, UTTERMOST, EXEPT and REACHING22). They are also underpinning Europe's prowess and leadership in applications and end markets.

In contrast, Europe's indigenous chip firms have currently given up on in-house MM wafer processing in favour of external foundries. As such, the local market for Europe's equipment and material's firms is already much reduced, offset by an increase in other geographic regions, primarily South East Asia.

If 450mm development does not take place in Europe, it is inevitable that Europe's equipment and materials firms would need to move these activities out of Europe closer to their customers with the knock on effect for Europe's research labs that now both their local indigenous advanced chip manufacturing and equipment and materials firms all had no 450mm European presence.

They too would eventually be obliged to shift these activities closer to where the market was, rendering programmes such as ENIAC and CATRENE irrelevant for Europe, simply becoming R&D subsidies for other world regions.

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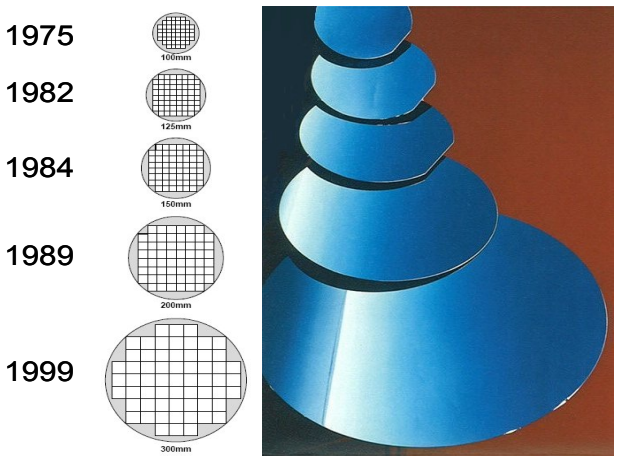
10. 450mm Cost Analysis

At the 200mm to 300mm transition there were a large number of advantageous factors justifying the expense of developing and making the transition, despite the large costs involved, Figure 9. As summarised below, some, but not all, of these cost components also improve with the transition to 450mm.

Figure 9 – Previous Wafer Size Transitions



Cost Comparison

200mm To 300mm Conversion

(At Maturity)

Cost Per Square cm	25 - 30% Less
Usable Portion of Wafer	3 - 14% More
Cost Per Chip	27 - 39% Less
Labor	About Equal
Tool Capital Cost	20 - 40% More
Materials Use	About Equal
Emissions	About Equal
Process/Probe Yield	Slightly Better

Source: TI (1996)

10.1. Increased Wafer Area

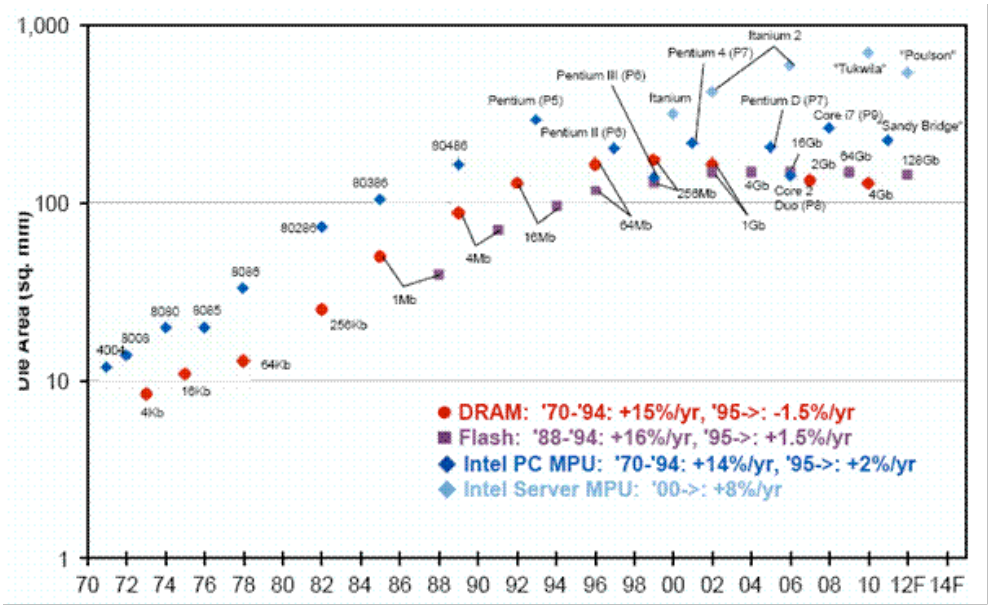
Cost benefit: Neutral to Slightly positive

At 200mm, for large die, there was a significant degree of wastage due to the areas known as marginal space around the circumference of the wafer where a whole die could either not be placed or was placed partially incomplete. This effect was reduced by the transition to 300mm and a similar improvement will be possible with the move to 450mm wafers. But, given there has been little overall increase in average die size over the past decade, Figure 10, the incremental benefit to be gained will be less. The gross number of die per wafer is determined by the formula:

$$DPW = d\pi\left(\frac{d}{4S} - \frac{1}{\sqrt{2S}}\right)$$

where 'd' is the diameter of the wafer and 'S' is the area of a single die. 'S' appears to have now stopped increasing and is in fact currently shrinking on memory products, and so the gross number of die per wafer simply increases in direct proportion to the area.

Figure 10 – Die Size Trends



Source: Intel

10.2. Substrate Costs

Cost benefit: Negative

The unprocessed wafers are thicker and so less will be produced per tonne of silicon crystalline ingot. The greater weight of the ingots also means they will take longer to cool and the increased thickness of the final processed die may mean an increased requirement for back-grinding. Sumco have even stated publicly their concern about the ability of the industry to produce cost effective 450mm substrates in volume. No other substrate manufacturers raised this issue during the interviews though.

10.3. Wafer Processing Material Usage Costs

Cost benefit: Neutral to Slightly Positive

The new equipment developed for 300mm offered more efficient techniques for the diffusion, lithography and etching processes over the older 200mm equipment. We do not expect to see such major improvements in the transition to 450mm and usage of materials and gases will likely be similar per die except for rare materials where 450mm chamber design may show a reduction of parasitic material consumption.

10.4. Wafer Processing Energy Usage Costs

Cost benefit: Neutral

The more advanced equipment required to produce new process technologies inevitably uses more power. However this would have been the same increase seen if these processes were ported to 300mm wafers. Far and away the biggest user of energy will be the EUV lasers which have phenomenally low efficiency ratings even at the end of their current development roadmap.

10.5. Wafer Processing Costs

Cost benefit: Positive (up to 2x improvement)

Here is the big improvement that the larger wafer size brings. Exposure of the resist is still performed using step and repeat techniques, so the time per die is constant, but every other process is on a per wafer basis meaning the cost per die drops proportionally to the area.

10.6. Wafer Handling Costs

Cost benefit: Positive (up to 1.5x improvement)

Anyone looking into a modern fab through the viewing windows is usually surprised to see just how few operators are involved. The move to 300mm wafers, with their inherent increased fragility, forced the industry to move from predominantly processing by hand to more automated handling but still requires a sizeable number of operatives.

Later generation 300mm fabs did improve this significantly with control being moved to an operations room but the introduction of 450mm is still seen as an opportunity to significantly upgrade the amount of automation within a fab. For example TSMC has stated that 450mm wafer technology will save it 7k jobs at the end of ten years compared with if it had remained with the 300mm size. Although hard to check accurately, we believe this represents roughly a 33 percent reduction in overall staffing levels.

10.7. Total Cost Per Finished Die

Cost benefit: Positive (up to 30 percent cost reduction)

It is expected that the transition to 450mm wafers will significantly reduce the overall cost per die, this being one of the three key driving forces behind the transition. In 1996 TI reported a 27-39 percent die cost saving attributable to the 300mm transition, Figure 9, which is in general agreement with other firm's experience. We do not expect die cost to decrease by quite the same degree, but the general industry expectation is for a 30 percent decline. Indeed this has now become part of the overall 450mm requirements specification.

Due to the significantly increased levels of automation – at 450mm absolutely everything has to be automated – the anticipated savings in labour costs will be considerably more, despite the slightly offsetting increase in the number of technicians required.

There were initial concerns that if EUV throughput speed does not improve, this may negate some of the 450mm cost benefits due to the need for quad-patterning etc. However,

interviews have shed light on the fact that the impact of EUV lithography on manufacturing competitiveness is strictly the same on both 300mm and 450mm platforms. Therefore it should be emphasized that if EUV throughput speed does not improve, this will give even more priority on 450mm to achieve die cost reduction.

11. Semiconductor Supply Chain Upstream Links

11.1. Material & Equipment Suppliers

The clustering effect, later developed in Chapter 13, is not a characteristic of advanced semiconductor manufacturing alone and similar knowledge concentrations apply upstream in the supply chain, due to the level of expertise necessary to meet the stringent constraints of advanced semiconductor manufacturing processes.

Many companies have already benefited from the state-of-the-art investments made by European-based IDMs in advanced process manufacturing in Europe, which has in turn helped them build and increase their market leadership abroad. These success stories demonstrate the strong linkages that exist between IDMs and their suppliers when it comes to advanced processes and state-of-the-art technologies.

A good example of clustering is ASML with its integrator business model under which 90 percent of its systems costs are externally supplied. The company works with approximately 500 suppliers worldwide underpinned by an R&D network of about 20k jobs, 35 percent (by product-related supply value) of which are located in the Netherlands, 45 percent elsewhere in Europe and the remaining 20 percent elsewhere. The ASML case is also interesting from a qualification perspective since R&D staff represent about a third of total ASML employees, with a large proportion of PhD and MSc in the total headcount.

R&D investment from equipment and material suppliers is heavily dependent on the most advanced semiconductor manufacturing facilities as can be seen by the equipment suppliers' R&D investment trend for successive wafer generations, Figure 7 (see §8.1). Were 450mm wafer manufacturing not to take place in Europe, much of the associate R&D spend would also not take place in Europe with the consequential loss of the economic value it leverages.

This concern was raised by SEMI in its October 2008 White Paper "6 Recommendations to the European Union and National Governments to Increase Europe's Microelectronic Industry Competitiveness", highlights that *"Although system integration, R&D and small scale production might still remain in Europe, SEMI Europe members fear that without major semiconductor manufacturing, eventually knowledge-based activities will also relocate to other regions"*.

If there was such a dislocation in the European equipment and material supply chain due to the lack of maintaining an advanced manufacturing presence in Europe, the repercussions would be serious and far-reaching. According to SEMI, SMEs account for 88 percent of the European material and equipment suppliers, representing a total of 105k employees in Europe. Without access to state-of-the-art manufacturing facilities in Europe, it would be extremely difficult for these SMEs to maintain their activities in Europe, if at all, when competing with large industrial groups with a global presence.

11.2. Research & Development

All the major clusters for advanced semiconductor manufacturing demonstrate strong synergies with the research community, including university and research labs, for example:

- Albany – CNSE
- Benelux – IMEC
- France – Leti
- Germany – Fraunhofer
- Taiwan – ITRI

The virtuous proximity between research infrastructures and advanced semiconductor manufacturing facilities has consistently shown to have played a key role in enabling new technologies to be implemented in product demonstrators in a quasi-industrial environment.

As many past success stories have shown, building a bridge between technological research and industrial manufacturing contributes to the industrial feasibility of research projects and can eventually lead to successful company spin-offs.

As Integration continues and miniaturisation reaches unprecedented levels of physics, the cluster coupling between advanced manufacturing and R&D infrastructure becomes even stronger. The availability of a first class research and academic infrastructure will become even more of a crucial competitive advantage for the next major phase of industrial investment. A European strategy for advanced semiconductor manufacturing would be able to build on the strength of this R&D leadership.

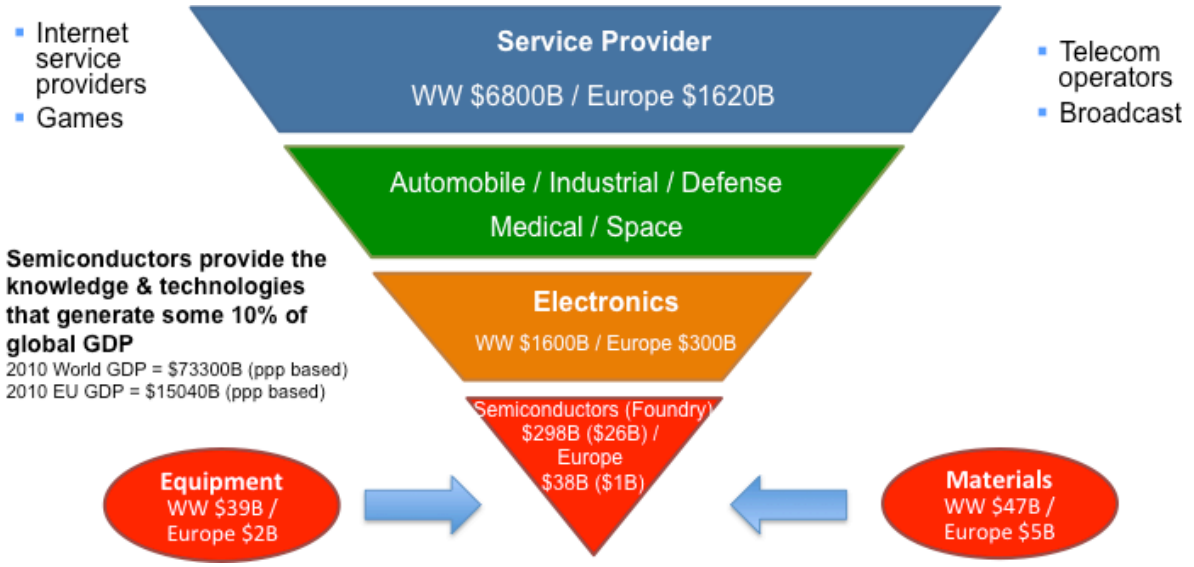
12. Downstream Links With End Systems & Services

12.1. Semiconductors Are An Enabling Industry

The ESIA in their 2008 Competitiveness Report stated *"Semiconductors are crucial to Europe's competitiveness. They enable 90 percent of the key technologies and innovations required for advancing a sustainable information and communication economy and directly contribute to generating approximately 10 percent of both European and worldwide GDP. Therefore, a vital semiconductor industry is essential if Europe is to remain one of the world's leading knowledge-based economies and realise the European Union's ambition of putting the Information Society at the heart of its strategy for the 21st century."*

The ESIA's strong statement recognises the very specific characteristics and leverage that the semiconductor industry has on the entire economy, Figure 11, and is in line with numerous other previous and subsequent findings including the: ESIA Reports (2005 and 2008); Aho Report (2005); ISTAG Report (2006); ICT Competitiveness Report (2006); ENIAC SRA Report (2007); CATRENE Whitebook (2007); Electra Report (2008); Rapport Saunier Report (2008); and Malier Report (2010).

Figure 11 – Economic Leverage Of Semiconductor Supply Chain



Source: DECISION, ESIA, Future Horizons, IMF, WSTS

It was also the key finding of the January 1995 "Report Of The European Microelectronics Panel" prepared by a panel of leading European executives from the whole value chain and to which Future Horizons was co-opted, (the so-called Cornu Report after the panel's chairman Jo Cornu, then Chairman of Alcatel) used by the European Commission and the various PAs to justify the establishment of MEDEA in 1996.

These reports all provide striking examples of the different types of downstream semiconductor industry leverage in the value chain including:

- New activity/service creation: for instance mobile communication and the development of Internet services
- Productivity gains in services, manufacturing and transport: through increased device and system functionality, system efficiency and communication capabilities
- Increased safety and security: for people (transport and residential), for goods (logistics, transactions and infrastructure) and also at the state level (defence, homeland security and space)
- Environmental protection and power management: thanks to ever more sophisticated monitoring and control systems either integrated in industrial facilities, infrastructures or embedded platforms such as transport

Finally, in its communication document *"Preparing for our Future: Developing a common strategy for key enabling technologies (KET) in the EU",* the European Commission acknowledged the key contribution of micro/nanoelectronics. The document states micro/nanoelectronics could be *"regarded as the most strategically relevant KET given its economic potential, knowledge intensity and contribution to solving societal challenges",* as also mentioned in the Tender Specification of this 450mm study.

It is now fair to say that there is a strong consensus in Europe that independent access to semiconductor technology is fundamental to securing the competitiveness of integrating industries, a message that Pasquale Pistorio has been preaching for the past 30 years since his return to Europe in the early 1980s to head up SGS-Ates, the then-ailing Italian chip firm.

12.2. Competitiveness Of Integrating Industries

In a cost driven industry, the differentiation between electronic OEMs increasingly relies on product functionality and, as a consequence, on semiconductor technology. For an electronic OEM, having access to advanced semiconductor technology allows them to optimize the product performances and differentiation whilst simultaneously keeping costs under control, which in turn directly contributes to its global competitiveness.

This interdependence between semiconductor suppliers and electronics OEMs has been demonstrated in many application sectors of the electronics industry, for example in the consumer industry in the 1980-90s, when Japanese OEMs displaced the European and US players thanks to the technological leadership provided by their local semiconductor suppliers.

Similar examples can be highlighted in Europe, where large European OEMs in the Telecommunication and Automotive industries consolidated their global competitiveness and market position thanks to strategic alliances with their European semiconductor suppliers, providing them with advanced access to the right semiconductor technology and solutions at the right time and cost, for example Nokia with STMicroelectronics for power management

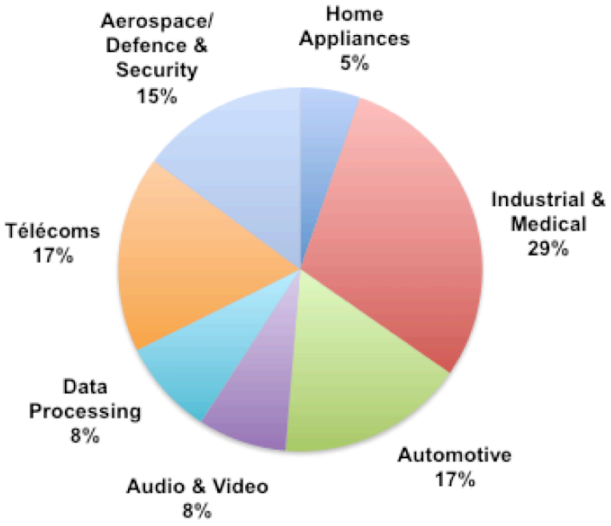
devices and Bosch with the German automotive industry for electronic injection control system.

More recently the success of Apple in the 3C market convergence (Consumer, Communication and Computing) relies on the firm's tight control over the design of embedded processors giving its products key differentiating features like superior power autonomy and user interface.

This virtuous cooperation and proximity between semiconductor suppliers and OEM integrators is even more strategic in markets that directly concern the sovereignty of nations such as the Aerospace/Defense and Security sectors, where exports control regulations are often implemented as a competitive tool favouring domestic industries against foreign competition.

A striking demonstration of the virtuous relationships between semiconductor suppliers and integrating industries is being provided by the strong correlation between European electronic equipment production (OEMs production in Europe) and European semiconductor industry competitive positions per application sector, Figures 12 and 13.

Figure 12 – European Electronic Equipment Production
(2010, Percent Of Value)

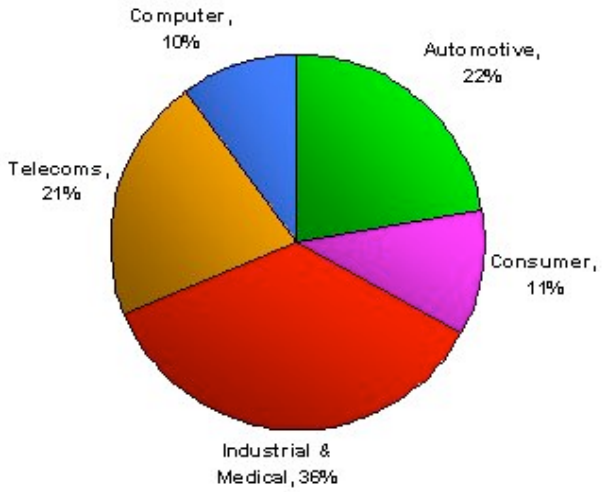


Areas of European leadership

Application sector	European share of World production
Automotive	**37%**
Industrial & Medical	**33%**
Aerospace & Security	**29%**

Source: DECISION

Figure 13 – European Semiconductor Sales By Application
(2010, Percent Of Value)



Source: Company Reports/Future Horizons (2010)

12.3. Manufacturing Crucial For Strategic Independence

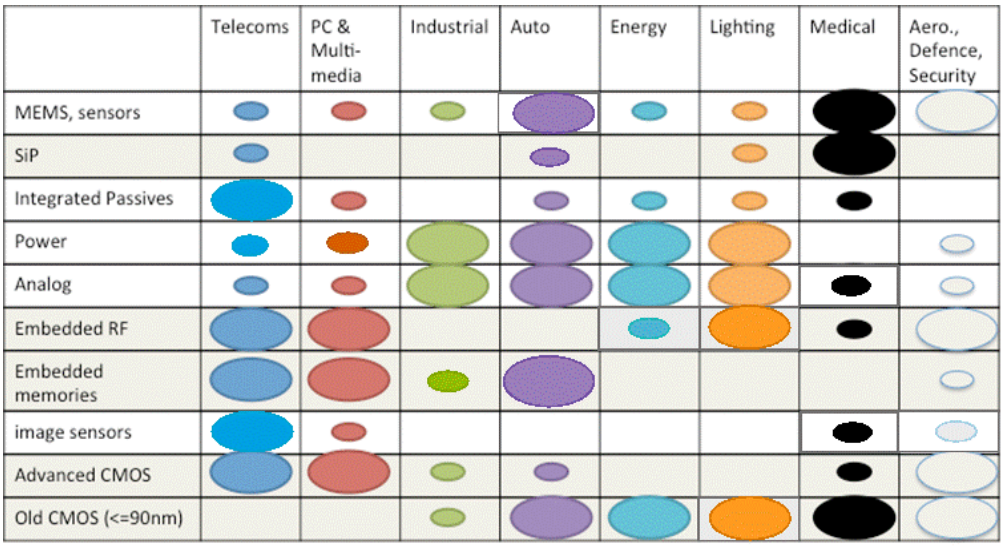
The semiconductor industry is one of the most capital-intensive industries in the world and is consequently exposed to several critical factors that can turn into risks downstream in the value chain. This includes the progressive consolidation and concentration of advanced semiconductor manufacturing base from both a geographical perspective and capital ownership perspective.

It has been shown that close proximity between semiconductor suppliers and the system integrators reduces time to market and increases the overall competitiveness of the industry. This is particularly true in Europe where semiconductor suppliers and integrators are heavily dependent on application-oriented products needing MtM specific technological integration capabilities. As a result, the need to maintain and develop advanced semiconductor manufacturing in Europe is a matter of ensuring its future strategic independence.

In fact, given the way society needs are developing, semiconductor manufacturing in Europe will become even more strategic since future innovation in domains like health, energy, security and telecoms will increasingly rely on semiconductors for advanced manufacturing integration and customisation.

Figure 14 illustrates the technological heterogeneity that semiconductor suppliers need to master in order to efficiently compete in the key vertical application domains whereby the large bubbles refer to key components in equipment/system and the small bubbles refer to secondary components in equipment/system.

Figure 14 – Application Segment By Semiconductor Technology



Source: CATRENE White Book, DECISION, Future Horizons, Malier Report (2010)

Some of these technologies, for example power, MEMS and sensors, can be considered as niche segments of the industry that do not follow the traditional Moore's law. However, mastering the integration of others (the grey area) relies at some point in time on the then current most advanced CMOS technologies.

In other words, it is only a matter of time before today's MM will form the base for tomorrow's MtM. Adopting a MtM strategy does not let industry off the MM hook, it just delays it. Failure to keep pace with MM simply buys a temporary stay of execution, not a reprieve.

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13. Economic Impact Of Advanced IC Manufacturing

13.1. Impact On Trade Balance

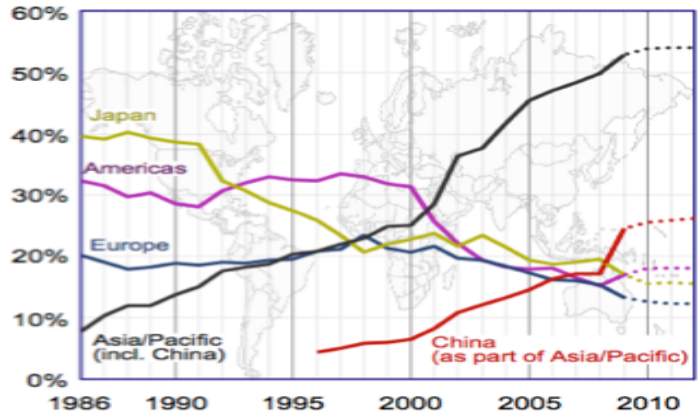
Industrial manufacturing activities are an essential pillar of the economy since sales of industrial products inject currency into the country of production (step 1). This in turn is both consumed within the country, creating jobs and services (step 2) and used to buy goods and services from abroad (step 3).

Clearly, if step 1 does not take place, then steps 2 and 3 will not exist unless alternative public support schemes are put in place instead, building up the national debt. A decline of industrial manufacturing at a national or regional level thus has considerable impact on future economic growth, as has already been experienced in many of the world's developed countries including Europe as currently shown by the Euro-zone crisis. In contrast, Germany's current strong economic performance in the post-Lehman economic crisis is attributed in part to its still strong and vibrant manufacturing sector.

As with other industrial manufacturing activities, advanced semiconductor manufacturing can contribute significantly to this trade balance mechanism given the fact that a large and growing proportion of these devices will be shipped to other regions. In fact, an advanced state-of-art semiconductor manufacturing facility could generate multi-billion dollars of export sales per year. Such a massive impact on the balance of payments can be explained by an increased consolidation of the semiconductor manufacturing industrial base, particularly at the most advanced technological nodes, but also by the semiconductor market dynamics.

In 2001 Asia/Pacific, which includes China, Taiwan and Korea, overtook the USA to become the world's largest semiconductor market, driven by the shift of electronic equipment production from the established economies to this region, Figure 15.

Figure 15 – Semiconductor Sales By Region, 1986-2010



Source: ESIA, WSTS (December 2010)

From under 10 percent of the total just 15 years ago, by 2008 Asia/Pacific accounted for over half of the world's semiconductor consumption, and is still rising.

Looking at the market shares by region, the USA has the highest ASP value, reflecting the higher-value end products in production there, and was the only developed economy to have not only maintained its unit production market share between 2008 and 2010 but at the same time managed to increase its ASP, and therefore sales value, as well, Figure 16.

Figure 16 – Regional Share Of Semiconductor Sales, 2008 & 2010

2010	Value ($bn)	Units (bn)	ASP ($)
Americas	53.7	52.3	$1.026
Europe	38.1	84.6	$0.450
Japan	46.8	89.1	$0.523
Asia Pacific	160.0	435.6	$0.367
China	63.1	218.6	$0.289
Total World	298.6	661.5	$0.451

Market Share	Value ($bn)	Units (bn)	ASP ($)
Americas	18.0%	7.9%	2.28
Europe	12.8%	12.8%	1.00
Japan	15.6%	13.5%	1.16
Asia Pacific	53.6%	65.8%	0.81
China	21.2%	33.1%	0.64
Total World	100.0%	100.0%	1.00

2008	Value ($bn)	Units (bn)	ASP ($)
Americas	37.9	44.7	$0.847
Europe	38.2	72.2	$0.530
Japan	48.5	94.2	$0.515
Asia Pacific	124.0	349.4	$0.355
China	45.1	169.8	$0.266
Total World	248.6	560.6	$0.443

Market Share	Value ($bn)	Units (bn)	ASP ($)
Americas	15.2%	8.0%	1.91
Europe	15.4%	12.9%	1.20
Japan	19.5%	16.8%	1.16
Asia Pacific	49.9%	62.3%	0.80
China	18.2%	30.3%	0.60
Total World	100.0%	100.0%	1.00

Region	Units	ASP	Value	Comments
US	=	+	+	ASP 2.3x World Average
Japan	-	=	-	Good But Not That Good
Asia Pac	+	=	+	ASP 0.8x World Average
China	+	+	++	Moving Upstream
Europe	=	-	-	Losing Value & Volume

Source: WSTS/Future Horizons (February 2011)

By comparison, Japan lost unit sales share but maintained its ASP value, thereby suffering an overall sales value market share loss in proportion to its unit share decline. In contrast, Europe held its unit market share but saw its ASP erode dramatically with the consequential loss of its value market shared.

Asia Pacific held its ASP value but increased its unit share, whilst within this overall region, China increased both its unit and ASP shares. Not surprisingly Asia Pacific has the lowest ASP value of all the world regions, reflecting its role as a global source of low-cost electronics equipment production. Interestingly China increased its ASP, outperforming the Asia Pacific average, reflecting its increasing role as a supplier of ever-higher quality and more sophisticated end products.

The economic significance of Asia Pacific now accounting for over half of the world's semiconductor sales should not be underestimated given that most of this is re-exported in

the form of finished electronics equipment with a typical 5x mark up at the end equipment sales value.

Even more tellingly is the fact that Europe semiconductor ASP is now right at the world average, ahead of Asia Pacific but behind Japan by approximately the same degree, a serious loss of value-add given it was at parity with Japan only two years ago.

13.2. Impact On Employment

In addition to its macroeconomic role, advanced semiconductor manufacturing also exhibits a large microeconomic leverage. Studies conducted to analyse the impact of semiconductor clusters in Dresden (DIW, 2002) and Crolles (Reverdy, 2007) point to the same conclusions. These studies have analysed in detail the impact of advanced semiconductor manufacturing infrastructures on employment based on three major mechanisms:

- The clustering effect that attracts to the vicinity of advanced semiconductor manufacturing infrastructure both suppliers and integrators with highly qualified employees

- The local redistribution effect due to the cluster activity itself and the local consumption of salaries, which creates locally induced employment in other economic activities (mainly services) covering the full spectrum of qualification

- The national impact, whereby the cluster industrial activity stimulates employment in other regions. This latter factor can be seen as a geographic extension of the previous ones

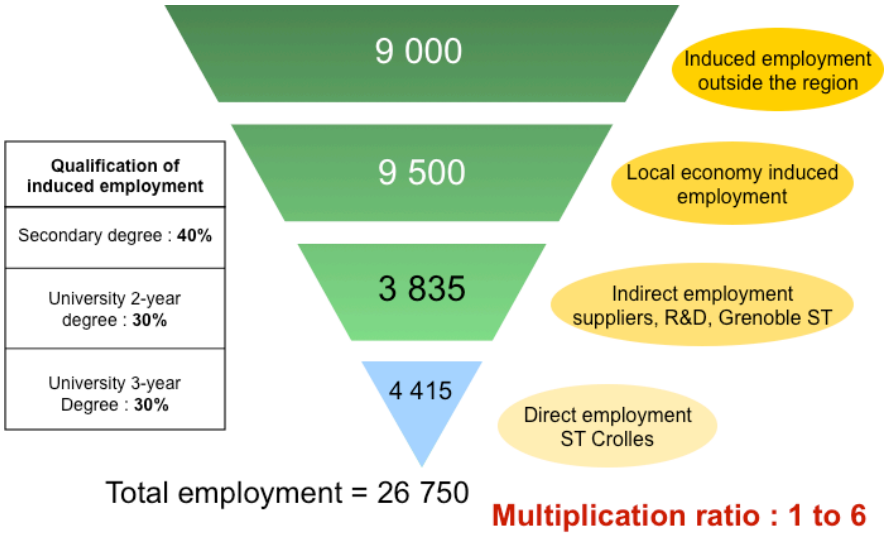
The study of the Grenoble-Crolles ecosystem from 1993 to 2006 showed that, taking all these effects into account, one job in an advanced semiconductor R&D facility generates at least five additional jobs within the economy with the following structure, Figure 17.

The Dresden study conducted by DIW in 2002 indicated that one job in Dresden's microelectronic operation sites (AMD + Infineon, 6300 employees in total) generated 0.7 jobs in the semiconductor supply chain (4183 employees) and 0.8 induced jobs in the rest of the economy due to the redistribution of salaries (4824 employees), leading to a multiplication ratio of 1 to 2.5.

Although the leverage on employment is significantly smaller in the Dresden case study, this result does not contradict the Crolles study outcome since the methodology and perimeter used are not strictly comparable in both studies. Indeed the Dresden study focused solely on industrial activities and is not counting the impact on research and education.

Whatever the multiplication factors are, these are still under-estimated since both analyses did not take into account the enabling role of the semiconductor industry downstream in the supply chain and the impact of advanced semiconductor manufacturing infrastructures on the competitiveness of integrating industries.

Figure 17 – Impact Of Employment, Crolles Case Study



Source: Reverdy (2007)

As indicated in the Key Enabling Technology Final Report, it is now globally acknowledged that: *"Mastering and deploying Key Enabling Technologies (KETs) in the European Union is central to strengthening Europe's capacity for industrial innovation and the development of new products and services needed to deliver smart, sustainable and inclusive European growth"*.

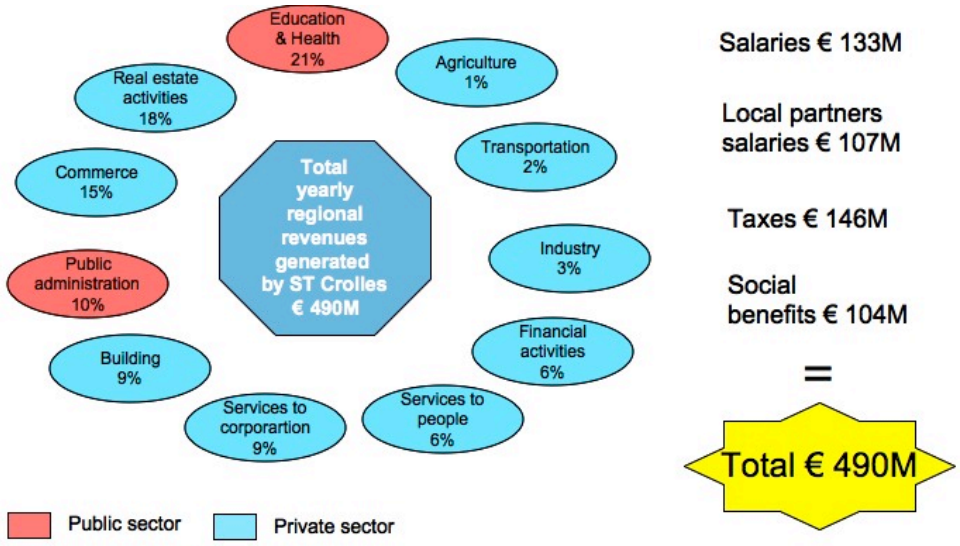
13.3. Return On Public Investment

History has shown that state-of-the-art clusters in any industry generally require a considerable level of private investment and public support. However studies conducted on clusters have estimated the ROI PAs can expect from their investment in advanced semiconductor manufacturing facilities will be potentially very large. On top of employment creation, the high tech ecosystem generates revenues, high salaries, taxes and social benefits, which represent positive factors for the territorial economic development.

Whilst the overall conclusions of independent studies unanimously point to the large payback for PAs, thanks to the additional taxes and benefits to the local economic development, the absolute value varies on a case by case basis, the most positive being a study undertaken by the State of New York in its study *"Assessing the Economic Impact of Attracting Semiconductor Industry"* (March 2008, Semico Research) where an ROI in excess of 200 percent over a five year period was estimated. Whilst the results of this study have been rejected by some taxpayer groups as too optimistic and inaccurate, it does place a peg in the ground at the most optimistic end of the claims. More directly applicable to Europe is the study on the Crolles and Dresden advanced manufacturing activities.

The Crolles case study concluded that that global revenue generated by Crolles fabs activity was €490 million per year for the Rhônes Alpes region as shown in Figure 18.

Figure 18 – Semiconductor Activity Regional Revenue Distribution



Source: Reverdy (2007)

Based on this analysis of revenues, the study also showed that the payback for local PAs was very large and rapid since the "Taxe Professionnelle" paid by STMicroelectronics for its Crolles site during the period 2002-2007 represented as much as €450 million, which is three times the public subsidies given to the Crolles 2 Alliance programme by local PAs. At the national level, the study estimated that Crolles industrial activities generated an annual income of €600 million per year.

NB. The "Taxe Professionnelle" was a tax linked to any professional activity in France that was based on land value and tangible assets. It has been cancelled in 2010 and replaced by the "Contribution Economique Territoriale", more favorable to industrial investment.

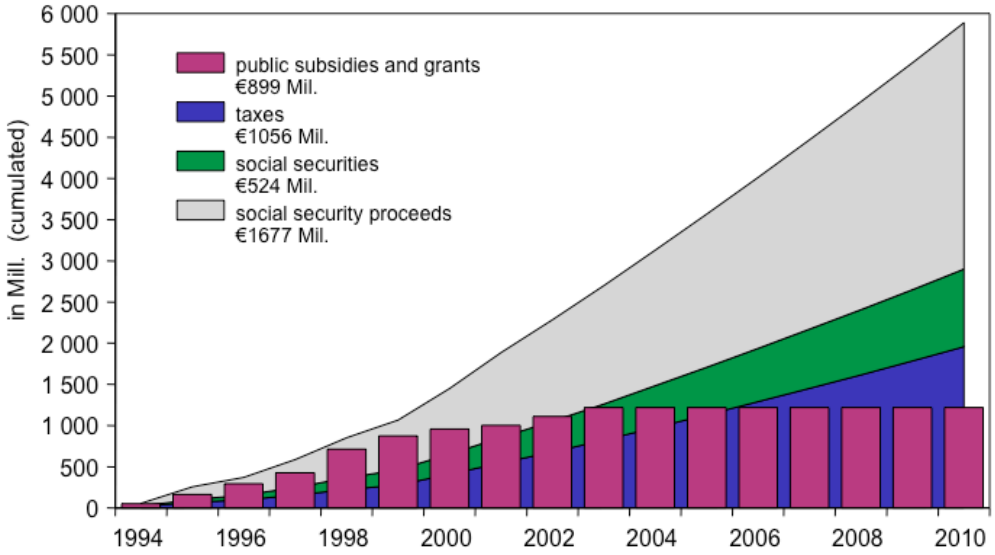
The Dresden study also provided in 2002 an analysis of PAs investment payback, based on the analysis of fiscal returns from Dresden manufacturing activities covering the period 1994 to 2010. Such an estimate was based on a projection of income from Infineon and AMD operations over the period, at discounted present value, and assuming no discontinuity in business operations, Figure 19. This model also excluded future developments such as the establishment of new companies, industrial activities or technological changes.

The calculation of fiscal effects indicates that the cumulated taxes paid to PAs exceed the amount of subsidies and grants in 2006. If the impact of social securities is considered (under-spending from PAs due to lower unemployment), then the breakeven point moves to 2003. Finally the additional revenue from social security proceeds reach a present value of €1677 million and would form the largest revenue item if the financial position of the social security system was taken into account. This would make the overall return on investment even more positive for PAs.

Again, studies on Crolles and Dresden ecosystem, despite different approaches, both lead to similar conclusions, indicating that the public support and promotion of the development of

state-of-the-art semiconductor manufacturing facilities tend to trigger a virtuous economic process providing not only positive but also fast return on public investment.

Figure 19 – Public Subsidies Fiscal Effects Of AMD & Infineon Investments (excl Fab 36)



Source: DIW (2002)

As already mentioned in the previous section, the Crolles and Dresden studies do not take into account in their quantitative assessment the impact of advanced manufacturing facilities on the competitiveness and innovation dynamics downstream in the value chain within integrating industries.

13.4. Summary & Conclusions

Advanced semiconductor manufacturing facilities have a positive impact on the global economy. On top of their enabling role and key contribution to the competitiveness of integrating industries, studies have demonstrated that such infrastructures provide a strong stimulus to local and national economies through employment creation and fiscal returns making it worth for PAs to support their development. State-of-the-art semiconductor manufacturing facilities also (rapidly) generate multi-billion dollars of export sales and could therefore significantly contribute to the trade balance disparity dilemma that is regularly pointed out as one of the major European weakness in the current debt crisis.

The ESIA Competitiveness Report (2008) concluded that concentration on the four pillars of R&D&I, lead markets, manufacturing and education is the way forward for the competitiveness of European industry. It also highlighted that the clustering effect in the semiconductor industry, initially driven by large companies, is now being strongly promoted

and driven by national and local authorities through advantageous framework conditions, with the aim to seize the aforementioned benefits of such centres of excellence.

In such a context, Europe's Industrial policy is currently benefiting from a renewed interest in manufacturing from policy makers, with a strong emphasis being given to the advanced manufacturing activities in selected Key Enabling Technologies (including semiconductor technologies) that are necessary to master innovation and meet future society needs, especially the ageing population, security and environment issues.

In its February 2011 Interim Report, the KET High Level Group identified several key benefits as the result of having an advanced manufacturing infrastructure in Europe, namely:

- **Time to Market** – acceleration of the learning curve on new manufacturing technologies and products in order to arrive amongst the first on non-mature markets with a high probability of penetration

- **Competitiveness** – the ability to absorb the enormous fixed costs of production on a volume sufficiently large enough to bring costs in line with its (notably Asian) international competitors

- **Independence** – retaining top-level production know-how and complete mastery of all the crucial KETs steps on European soil together with control of the whole product life cycle, from resource efficient and energy saving production to recycling processes

- **Supply Chain Links** – developing an efficient and modern industry and infrastructure for equipment, advanced manufacturing systems and the most advanced manufacturing technologies (machinery, processes, software and services) thereby generating a source of export revenues; the expertise to build high technology manufacturing facilities in Europe; and the ability to develop and improve existing manufacturing systems

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14. Public Support For Semiconductor Manufacturing

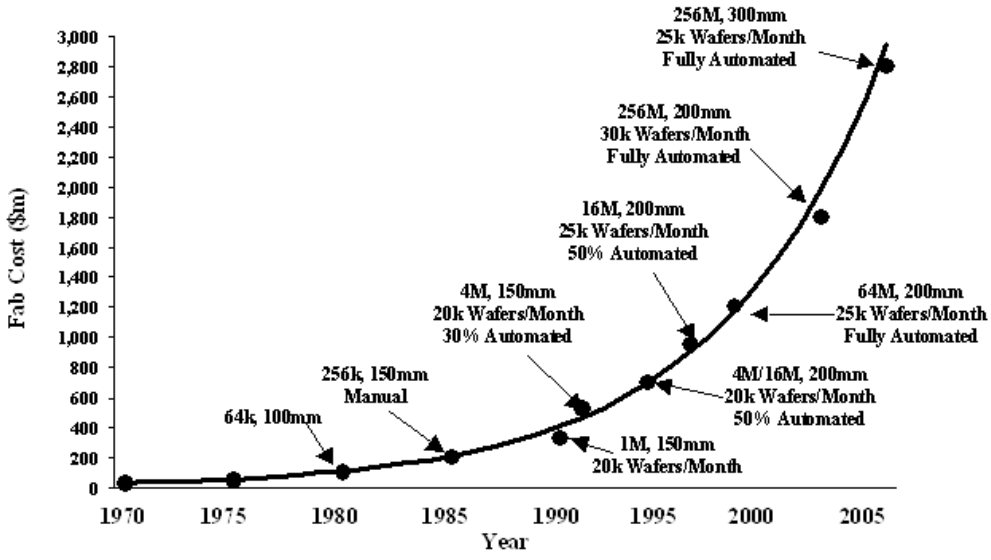
Given the fact that this topic is highly commercially sensitive, very little quantitative information on global public subsidies to the SC industry have been publicly disclosed. To make things worse, such information when it is published is generally rather vague and needs to be carefully validated and 'interpreted'. The information presented in this chapter has thus been predominantly derived from the Task 2 interviews with companies and PAs across the world on their expectations and experience.

14.1. Introduction

The semiconductor industry is at the centre of fierce competition worldwide, not only between private companies but also between countries or territories. Several governments have adopted aggressive strategies to support the development of their national suppliers and encourage foreign direct investment in the sector, thus securing their innovation capability at the product, system and service levels.

However the real problem with semiconductor manufacturing is the growth in cost of a fab as shown in Figure 20 below. This graph roughly follows both the total size of the market and the complexity of an individual IC. Whilst some form of subsidies have always existed, from the late 1980s the sums involved moved beyond the reach of venture capital and governments had to become seriously involved in supporting the costs if they wanted fab plants in their country.

Figure 20 – Semiconductor Wafer Fab Cost Trends



Source: Future Horizons

Initially subsidies were made as direct grants but over the last two decades many regions have implemented strategies based on several instruments and schemes including:

- Fiscal incentives, for example tax, salaries, R&D tax credits, depreciation and infrastructure development
- Land acquisition, new roads and infrastructure
- Equipment funding, including capital grants for buildings and manufacturing equipment
- Utilities, for example energy cost subsidies
- Employee training programmes
- R&D funding

One of the goals of this Report was to try to compare the value of the different support structures offered by the different regions and separate myth from fact. Part of the interview process looked at the direct and indirect subsidies available worldwide for large investment projects. It also looked at support for R&D, the results of which are dealt with separately in Chapter 15.

14.2. Worldwide Public Subsidies of Wafer Fabs

As the degree of factory automation increased, the number of staff employed by a fab never increased commensurate with the fab size and investment cost to the point whereby it started to become politically unacceptable in most countries to maintain the level of support to the semiconductor industry as there are many other industries competing for the same value of support but offering far more actual jobs.

The level of subsidies on offer to attract wafer fab investment in Europe consequently decreased from 35% of the total investment cost during the period 1990 to 1997, to an intermediate level of 20% between 1998 and 2001 before finally reaching a modest 10.5 percent since the last modification of the EU state aid regulation in 2002.

Another prime example of this is mainland China which once had the goal of being a major player in semiconductor manufacturing but now prefers to place public investment in aerospace technologies and, to a lesser extent, PV plants.

Similarly, whilst Japan has recently given support to some of its LCD plants, in order to maintain its competitiveness here with Korea, and offers targeted R&D support to its semiconductor industry, it is known not to be willing to subsidise production fabs. This has forced many Japanese semiconductor firms to both merge and adopt a ‘fab-lite’ strategy, a far cry from their 1980’s hay-day when Japanese chip manufacturing was the envy of the world.

In the past Israel has supported Intel with US$1.2 billion of subsidies towards an inward investment of US$7.3 billion, a 16.4 percent subsidy, but the latest expansion of Intel’s Kiryat

Gap fab received only US$210 million towards its US$2.7 billion cost of upgrade, roughly half the level of previous support. Discussions were also held on locating a 450mm fab there but the government took the stance that in order to secure a subsidy the fab was built at another location. We presume this was to try to keep the 300mm fab running in parallel but it seems to have instead encouraged Intel to look elsewhere.

In Taiwan, the ITRI research operation and government funded spin-off scheme has created the highly successful TSMC but also the barely profitable UMC and a significant number of deeply unprofitable DRAM suppliers. To become profitable these companies require complete modernisation of their fabs at a cost they could never afford. Quite what the Taiwanese government will decide to do here remains one of the big unanswered questions.

Another aspect of Taiwan is the fact that the government does not levy taxes on fuel and also has a price stability mechanism which means their energy costs are one of the lowest in the world. Whether this actual constitutes a subsidy, however, will vary from year to year.

Singapore offers the highest R&D subsidies in the world and also offers land support for manufacturing operations together with tax breaks under its Pioneer status scheme. This is traditionally given to high-tech companies that introduce high-tech skills to the economy and entitles them to exemption from corporate income tax for a period of up to 15 years. There are also no withholding taxes levied on dividends, instead these are taxed at the standard rate with a tax credit being given for any corporate tax levied on the profits out of which dividends are paid. We could not identify any recent direct subsidies with no identifiable money having been paid to support the expansion of STMicroelectronics' fab there.

Korea's case is possibly the most complex in that the banks make cheap loans to semiconductor companies on the direction of the government. Hynix in particular has benefited from these several times in the past. It has also had local taxes and infrastructure charges waived. Koreas is thus one place where we found large subsidies continuing. However all support goes only to Korean companies so it is not possible for non-Korean firms to gain a financial advantage by setting up shop there.

In the Middle East, the Abu Dhabi national investment company, Advanced Technology Investment Company (ATIC), is the owner of GlobalFoundries who, despite fierce opposition and legal cases, is receiving US$1.4 billion from the State of New York – 30 percent of the Albany fab investment cost[1], and US$310 million from Germany – 10.5 percent of the total Dresden fab expansion cost which is the maximum support available for large investment projects in Europe based on the current state aid regulation. Its original strategic vision of building a state-of-the-art 450mm production fab in Abu Dhabi has recently been put on hold 'due to the current economic uncertainty'. More likely it has been kicked into the long grass due to the fact there is no existing semiconductor infrastructure there and almost every worker and engineer would need to have been brought in from Europe or the Far East and the difficulties of doing this would have made the plant impractical.

Whilst the companies and PAs we interviewed were generally unwilling to discuss this issue in much detail, at least on the record, by interrogating company reports and reading government papers, we were able to come up with the following overall summary which receive a tacit 'nod of agreement' when shared with knowledgeable sources.

[1] The current scope of Global Foundries Fab 8 project in Albany includes a total capital budget of approximately $4.6 billion for Module 1, Phase 1 and the Phase 2 shell.

- Fabs create a near constant number of jobs, despite the fact the investment cost rises exponentially but their increasingly high-level nature and the associated influx of skilled workers does create sizeable additional local wealth through secondary mechanisms

- Almost all new fabs will be built in locations close to existing fabs. The costs of adding all new infrastructure and supplier networks to support a new fab site are dissuasive

- In addition to up-front subsidies it is expected that additional support throughout the life of the fab will be available through mechanisms such as R&D support, utility subsidies and tax holidays

In conclusion we believe that Europe can compete with other locations for new fab plants provided it makes some changes to the system of support which currently limits public support to 10.5 percent for large investments and improves its availability of suitably educated engineers. It also needs to make sure that the same rules on subsidies need to apply uniformly across Europe no matter where the location.

It should also focus its efforts on supporting viable existing locations rather than use subsidies to promote a new region, as with Israel.

14.3. Technical Education

Talking to chip companies on what they looked for when choosing a fab site, whilst subsidies were important, a far more important issue to most was the availability of suitably educated staff. For example:

- TSMC stated that the lack of manufacturing-focused PhD engineers in Europe was a leading reason they would probably not base a 450mm fab here

- The Irish PA noted that its best engineering graduates were still going into banking even after the recent problems

- Intel advised it now has to recruit from further and further afield, to the East of Europe, to fill all its vacancies

- Most equipment manufacturers stated that recruiting the right staff was a constant problem

- Conversely the research institutes found recruiting students relatively easy, as did science and engineering departments in top universities, however we estimate that roughly 50 percent of the recent originate from outside the EU

These findings are also in line with a statement in the report of the HLG on KETs: *"Here the goal is to create a future world class cadre of engineers and technologists to ensure*

European competitiveness. Europe should produce at least one world-class research engineer or technologist for every fundamental research scientist. A significant rebalancing of output is required to underpin the innovation called for in Europe 2020."

The wording here is a little unfortunate in that it could imply having less research scientists. We assume what it was promoting was the need for more engineers and technologists without reducing the number of research scientists in which Europe is already deficient and having to recruit significant numbers from outside the EU.

Research scientist and research engineering are also rather different things. Science of its essence often has no targets, timescales or end-goals, and this attracts a certain sort of person. Conversely engineering, even in R&D, is all about targets and timescales. This attracts a different sort of person who tend to be more prestige and money-motivated. The fact that the electronics and semiconductor industries do not pay 'star' salaries to its top engineers in the same manner as e.g. the financial sector, software and pharmaceuticals is therefore part of the overall shortage problem.

In any case the ongoing problem for manufacturing in Europe is that those qualified to PhD level in Europe are rarely interested in manufacturing. Addressing these issues must be an integral part of Europe's 450mm strategic vision.

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15. Impact of R&D Funding

15.1. Semiconductor Industry R&D Funding Rationale

Like other funding instruments, R&D funding is a part of the competitiveness equation in the semiconductor industry as illustrated by the following case study for the mobile phone industry. Innovation in the mobile phone industry mostly relies on semiconductor suppliers who allocate between 10 and 20 percent of their revenues to R&D, enabling the development of a much larger mobile service market representing over 20 times the revenues of mobile chip suppliers. Telecom operators, who only invest 1 percent of their revenues in R&D, are thus benefiting from the semiconductor industry R&D intensity to create value and profits downstream in the supply chain.

Thus, the innovation in mobile phone technology also benefits the population through productivity gains and services, although none of the downstream beneficiaries pay any royalty to the component suppliers who are the originators of the innovation. Governments also collect taxes on these activities, again at no cost, resulting in numerous downstream benefits not being attributed to, or captured, by the company performing the initial R&D.

Since these firms cannot directly enjoy a share of these downstream revenues in the value chain, and are obliged to finance their R&D out of their own revenues, component suppliers would consequently be forced to under invest in R&D were it not for the fact they had access to various external funding programmes.

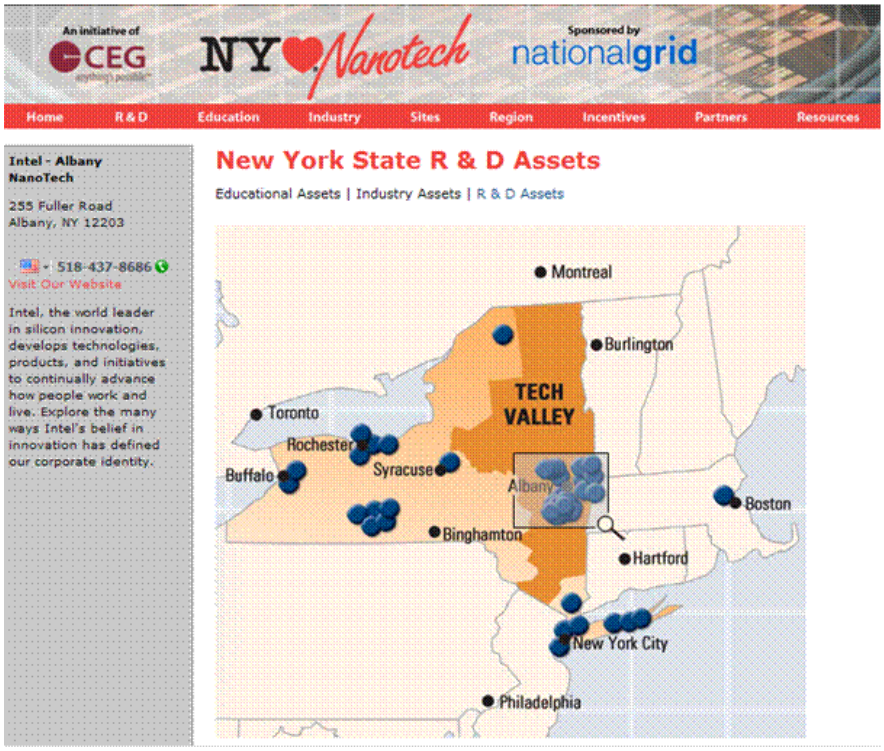
15.2. Competitive Landscape

In the USA, the State of New York has been funding Albany, the State's capital city, over the past five years in order to consolidate IBM's competitive position and attract foreign investment to the region. This included grants to enable Albany University to purchase the most advanced semiconductor processing equipment in order for it to set up a state-of-the-art process line for industrial research activities.

As a result, Albany is now the world's largest cluster for advanced semiconductor research, Figure 21, attracting investment from (in alphabetical order) AMD, Applied Materials, ASML, Dupont, IBM, Infineon, Intel, Micron, Renesas, Samsung, Sematech, STMicroelectronics, TEL, TI, TSMC and many others, Figure 22.

Ironically, Albany, originally named Beverwijck, is one of the oldest surviving European settlements from the original thirteen colonies and the longest continuously chartered city in the USA. It is now head to head in competing with IMEC and other international more specialist research establishments such as Leti, Fraunhofer and ITRI in the field of advanced semiconductor research and 450mm deployment.

Figure 21 – NY State Technology Cluster



Source: New York State Department of Economic Development

Figure 22 – Albany Cluster Partners

Source: New York State Department of Economic Development

During the course of our research, comments were made to the effect that Albany was being supported by 'billions of dollars' of public money. Our investigation into these suggestions revealed the following results:

- We have identified direct Albany funding of research on semiconductors, including but not limited to 450mm technology, of US$350 million to date
- An additional investment of US$100 million per annum is promised from now on, with 25 percent of this ring-fenced for 'energy saving technologies' though of course this can still be applied to doing so in 450mm fabs
- Many Europeans we meet think the number is much higher, but Americans we discuss this with were horrified it was so high. They had been assuming it was half to a quarter of the numbers we identified
- The university itself has its own sources of non-public funding and is active in its own right as a Venture Capitalist
- US$3.6 billion of the latest US$4.4 billion announced is coming from IBM over the next four years. The company is registered in NY State and so can claim R&D credits on this, as can GlobalFoundries. Intel however cannot as they are out of state registered
- There is huge outrage at the amounts of public money going to Albany and we were told if the Republicans win the next elections they will try to find ways to prevent NY State (a Democrat stronghold) continuing with the US$100 million per year investments
- The participation of foreign companies such as TSMC and ASML at Albany is causing a lot of disquiet, even though of course Qualcomm and Broadcom depend 100 percent on TSMC and the whole industry depends on ASML

Moving on to Asia, in addition to support and funding schemes dedicated to the infrastructure (buildings, land and utilities), manufacturing, tax regimes and customs activities, the region also gives priority to R&D funding in order to attract and build a world class semiconductor industry cluster environment. This includes tax credit schemes up to 150 percent of R&D expenses, covering new product development as well as manufacturing technology development.

In Europe the impact of R&D funding has been particularly important for the semiconductor industry, starting with the JESSI pre-competitive programme in 1989. Originally targeted to help Europe catch up in processing technology with its Japanese and US competitors (Korean and Taiwan at that time were not serious industry players), by the time the MEDEA follow on programme started in 1996, Europe had not only closed the technology gap but was starting to show leadership in both advanced system applications and technology clustering.

Co-operation within the European semiconductor supply chain on pre-competitive R&D projects now represents a huge European asset and has been copied to various degrees of success by the US (Albany) and Asia, especially Taiwan.

15.3. Current Status In Europe

There are currently four sources for R&D funding to the semiconductor industry in Europe namely:

- National funding including research infrastructure
- Regional initiatives, local development funds and clusters
- Trans-national EUREKA platforms e.g. CATRENE
- European Commission Framework Programme (currently FP7 and coming Horizon 2020) and Joint Technology Initiatives e.g. ENIAC

The largest European single cluster investment to date is the Nano2012 initiative in France where around €2.3 billion will be invested over five years in the Grenoble region, of which €457 million will come from the PAs.

The European Commission is currently increasing its funding to cooperative R&D projects through its ENIAC programme, Figure 23.

Figure 23 – Annual Public Funding To ENIAC Joint Technology Initiative (JTI)

(In million euros)	**2008**	**2009**	**2010**	**2011**
Actual Costs	211	248	201	374
National funding	62	66	54	85
EU funding	35	41	34	62

Source: European Commission

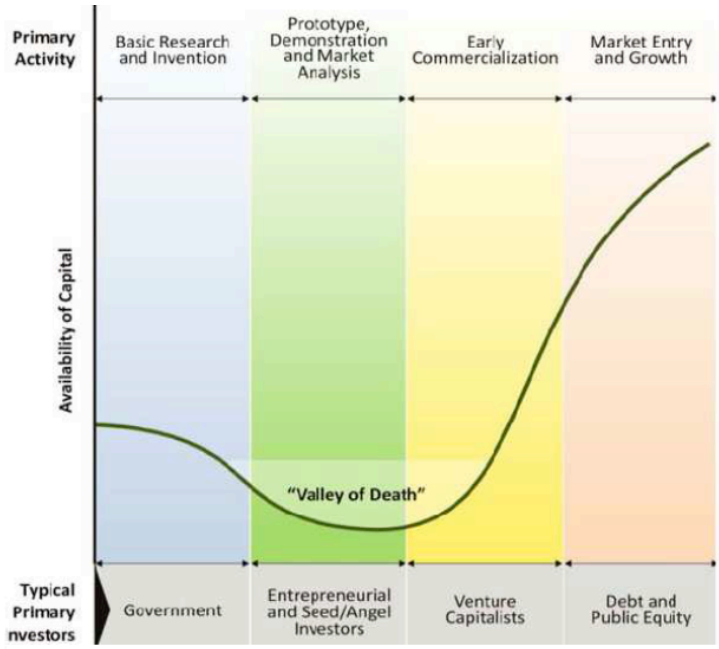
Finally, the CATRENE Eureka cluster also receives around €120 million funding from the PAs, down from a peak of over €180 million in the MEDEA+ programme. Including the investment from the companies involved in the corresponding projects, the total amount of R&D financed through CATRENE represents around €300 million to €400 million.

Despite this relatively high level of funding and European expertise in R&D co-operation, Europe has been losing ground with respect to its international competitors over the past decade due in part to the absence of a common European strategy and poor co-ordination between the various funding sources. According to the KET HLG Interim Report, 60 to 70

percent of R&D is not eligible for funding in the EU due to an inconsistent country to country interpretation of the eligibility criteria and tax credit systems for R&D activities.

Another key challenge for European R&D is its historic difficulty in bringing research to the market, the so-called Valley Of Death, Figure 24, and the lack of an innovation policy and framework to provide a bridge from basic research to pre-commercial products.

Figure 24 – Funding "Valley Of Death"



Source: European Commission KET Report (February 2010)

In a 2005 study by Inno AG *"Effectiveness of R&D to increase the competitiveness of Europe industry in the sector of Micro/Nanoelectronics"*, one of the key conclusions was that industry competitiveness was highly dependent on geographic proximity of the research with the market.

The KET initiative has now definitely put the overall objective of bringing research to market and production at the top of the European Commission agenda. This new ambition will set the trend for the new forthcoming Horizon 2020 strategy and all of the other initiatives mentioned above.

15.4. Current Outlook In Europe

In this context, the priorities should be to define and implement a common European strategy on industrial policy and a homogeneous set of supporting framework conditions with respect

to state aid and geographic restrictions. New funding instruments are currently being investigated in Europe, such as the Pre-Commercial Procurement programmes, in order to create the necessary bridge between research and end market and achieve critical mass at the European level.

16. EU SC Industry Position On 450mm

The purpose of the following chapter is to provide the reader with a synthesis of the current industrial, political and strategic context in Europe with regard to the 450mm transition. It is meant as an introduction to the subsequent scenarios chapter (see Chapter 17).

16.1. 450mm Semiconductor R&D In Europe

Undertaking a successful 450mm transition, and possibly also enhancing existing 300mm technology, will require the right balance of R&D and academic assets. Transistor design, process and other issues related to the transition to 450mm wafer size will also play a crucial role, as too will some specific areas of EDA tooling.

The interviews and background research analysed Europe's strengths and weaknesses in great deal and the following SWOT chart, Figure 25, was produced. Whilst it is natural that not everybody will agree with all of its conclusions, the team are confident it represents the reality of the situation.

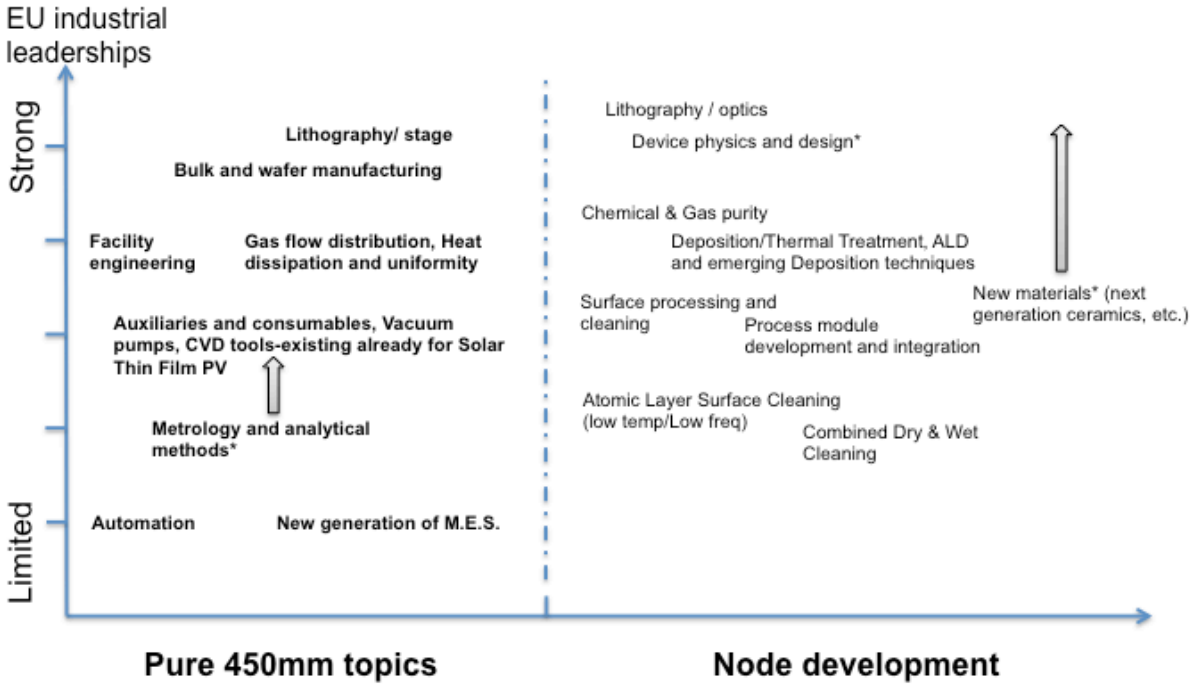
Given research by itself is of little use unless commercially utilised, Europe's strengths and weaknesses in research industrialisation were also analysed, Figure 26.

Figure 25 – European R&D SWOT

Strengths (strongest first)	Opportunities
❑ Lithography – optics and stage ❑ Device physics, Device design ❑ Device variance calculation, Standard cell design ❑ Bulk & Wafer manufacture, especially SOI ❑ Deposition/Thermal Treatment, ALD and emerging Deposition techniques ❑ High purity Chemicals and Gases ❑ New Materials such as Graphene, Ceramics & Lo-k materials ❑ 3D technologies such as TSV ❑ Facility Engineering ❑ Advanced process control ❑ Process Module Development/Integration ❑ Auxiliaries (e.g. vacuum pumps) ❑ Other Consumables ❑ Surface Processing and Cleaning	❑ E-beam lithography ❑ Mask technologies for EUV ❑ Nano-imprinting ❑ Post CMOS – carbon based route (US mostly going with silicon based route) ❑ Quantum devices ❑ Resist cleaning after implant
Current weaknesses (weakest first)	**Threats**
❑ Memristor based technologies (despite EU FP7/ENIAC funded projects) ❑ Fab Automation ❑ New generation of M.E.S ❑ Atomic Layer Surface Cleaning ❑ Combined Dry and Wet Cleaning ❑ Metrology and Analytical Methods ❑ Mask making	❑ Lack of consolidated European plan ❑ Risk that the G450C in Albany makes CNSE the dominant place in advanced process development ❑ EUV lasers don't meet development timescales ❑ Japan government backing for alternative EUV solution ❑ Lack of suitably qualified engineers in Europe ❑ Delays in funding by PAs ❑ Other funding issues as identified by KET

Source: Future Horizons/DECISION

Figure 26 – European Industrial Strength



16.1.1. European R&D Strengths

Europe clearly has a leading position in semiconductor technology and process R&D, with Belgium-based IMEC the recognized world leader in new semiconductor structures and processes, supported by the Leti and Fraunhofer institutions. IMEC has R&D contracts with almost every major semiconductor company in the world, including Intel, Samsung and TSMC, the three companies most likely to establish the first 450mm wafer fabs. It also benefits from having a robust advanced foundry solution in place with TSMC.

IMEC is also partnering in semiconductor lithography R&D with the world leader, ASML where their combined patent portfolio is now incredibly strong. So strong in fact that IMEC and ASML are unique in having the ability to make or break the photolithography capability for all future nodes. It is worth mentioning that tool assessment and selection is still performed internally by chip suppliers, with IMEC focusing on advanced process development.

Complementing IMEC's focus on advanced process technologies and consolidating Europe's pre-eminent position in this field, are two other major European research establishments, namely Leti in France and the Fraunhofer Institutes in Germany. Leti has a strong partnership with European companies, such as STMicroelectronics through its Crolles fab plant and Soitec specialising in SOI technologies but also with the IBM Alliance in Fishkill and Albany. It is also one of the world leaders in electron beam lithography, a complementary approach to EUV lithography developed at IMEC.

The Fraunhofer Institutes have many other specialities, notably in the area of advanced semiconductor die packaging and other disciplines that may play an important role in 450mm

transition such as automation and metrology.

All three establishments are members of numerous European Commission funded nanoelectronic research projects, the most relevant to this study being the EEMI450 programme and the CATRENE programmes relevant to the 450mm area.

16.1.2. European R&D Weaknesses

Despite Europe's undisputable wealth of R&D experience, it is failing in capitalising on this, as again reiterated in the February KET Report. Whereas in the 1990s European companies leveraged this R&D to attain strong positions in the global supply of semiconductors and equipment, since the turn of the decade, with relatively few exceptions, there has been a dearth of European companies willing to commercialise this research fully at the most advanced nodes.

Another issue frequently raised is that European funded research within the three main institutes is often too diverse with all three included to varying degrees on many projects. There may therefore be opportunities for better coordination here.

16.1.3. European R&D Threats

Europe led the 300mm transition, including equipment and process R&D via its Semiconductor 300 initiative, and could easily have done so again at the 450mm level given many of the key 450mm technologies have been developed in Europe. Unfortunately the indigenous European semiconductor companies were not minded to so do, possibly not helped by the lack of targeted funding to consolidated their manufacturing position.

Unfortunately, during the 300mm build out in the post dot com bust era, a wave of opinion grew in Europe that manufacturing was not of strategic European importance, culminating in the bankruptcy of Qimonda due to the lack of short-term financial support. This collapse and subsequent closure robbed Europe of its most advanced high-volume fab. Prior to this, STMicroelectronics' 300mm megafab in Catania had been shelved once the fab building and utilities were completed, with the facilities now used by 3Sun (Sharp/ENEL/ST) for PV solar production.

This lack of interest allowed CSNE at the University of Albany instead to make the required 450mm strategic investments, establishing it as the world's prime research establishment for the 450mm transition. CNSE, not Europe, will thus now be in the 450mm transition driving seat for the whole semiconductor industry. The upside of this is that it should result in a more homogeneous transition compared to 300mm, with everyone working to a common agenda. If therefore Europe chooses to build a 450mm fab, it will have no choice but to work with Albany on whatever 450mm initiative it may ultimately choose to make.

16.1.4. Other R&D Issues

Two notable exceptions from IMEC's process development partner list are IBM and STMicroelectronics, although they have both previously partnered with IMEC in other areas

of research. At the time of its formation, IBM's R&D capabilities were intended to drive the Common Platform Alliance to process world dominance but this has so far not been achieved. The Alliance's choice of gate-first technology for the 32/28nm node has made it more difficult for the Alliance to evolve to the gate last technology needed at 22/20nm. Despite this, the Alliance is claiming they will have 20nm in 2012, 14nm in 2014 and 11nm/10nm in 2016 and TSMC are making similar claims.

This now sees IMEC orchestrating a common research effort at the most advanced nodes with Samsung (member of the IBM alliance), Toshiba, TSMC, Intel and most recently GlobalFoundries, another Common Alliance partner, indeed one that got quite badly burnt by the 32/28nm gate first decision.

One has to note however that the only European IDM involved in MM advanced R&D and the IBM Alliance, namely STMicroelectronics, is not participating to the common research effort led in Europe by IMEC on advanced nodes development. Further coordination in Europe is necessary to address the 450mm transition and we believe STMicroelectronics should be a key part of this coordination.

16.2. Current 450mm Dilemma In Europe

16.2.1. Industry Positions

For IC suppliers, while STMicroelectronics is positive about 450mm on the longer term and confirm the need for such a technological base by the end of the decade, it has in the short and medium term other priorities requiring substantial levels of resources on 300mm platforms (3D transistors, EUV and/or electron beam lithography). For the other indigenous IDMs in Europe, there is currently no interest or commitment to 450mm.

European Equipment and Material suppliers have a radically different approach and see 450mm as an opportunity to either consolidate their market position or capture additional market shares. Their main concern is currently to invest the right resources at the right location and the right timing so that they can seize the 450mm transition opportunity to increase their market share and actively participate to the coming consolidation of the equipment & material supplier industry.

As far as R&D institutes are concerned, the European landscape is very much scattered, due to their different business models and strategies, with IMEC strongly supporting 450mm so that the European leadership in advanced nodes development be secured, Fraunhofer willing to cooperate on selected issues like metrology and Leti prioritizing 300mm development, 3D and mask-less lithography instead. This difficulty to reach a common consensus in the European semiconductor industry on the 450mm wafer scale-up is aggravated by increased nationalism in Member States' industrial strategies over the recent past.

The 450mm transition will require very significant levels of investment and funding compared to the investment patterns for 300mm. The semiconductor industry will first require funding to develop 450mm tool sets and materials, with the total cost of this transition estimated at between US$25 billion and US$40 billion up to the time when the early adopters open their first 450mm volume fabs, possibly as early as 2018.

Once such a transition has been realized, funding will also be necessary to attract wafer fab investment. Such support is likely to represent total subsidies in the range of US$1 billion to US$3 billion based on wafer fab configuration (see Chapter 17) including both up-front subsidies and on-going incentives cumulated over the life of the fab (up to 10 years).

The capability of Europe to first play a role in the transition and ultimately host 450mm fab(s) will thus be conditioned to two factors, namely an industrial commitment to 450mm in Europe and a significant degree of coordination between all funding instruments available at local, national and community levels. The lack of a common EU strategy is thus currently a strong limitation to any European initiative. Collective effort in this field will be needed to make a successful 450mm transition.

16.2.2. National PA Positions

Six national PAs were interviewed within the scope of this study including Austria, Belgium, France, Germany, Ireland and the Netherlands. Those consultations raised several areas of convergence although their positions with regard to 450mm remain predominantly driven by their national industrial base requirement.

Among the convergence points is the recognized lack of a European long-term vision for the semiconductor industry and more specifically for semiconductor manufacturing in Europe. Such a shared vision at European level could then be translated by the industry into precise objectives and timings, which would subsequently be a base for the alignment of current funding policies and instruments. This could/should include new rules enabling the funding of large investments now required to remain competitive in the global world competition (matching clause, KET pilot lines, transnational funding, etc.).

Despite these lines of convergence, the 450mm transition remains a real chasm among national PAs between those supporting the transition including Ireland, Belgium and the Netherlands, all having industrial champions with proven business cases and commitment to 450mm, and those remaining hesitant or reluctant like Austria, France and Germany.

The latter are currently adopting a cautious attitude towards 450mm wafer scale up with participations limited to existing 450mm cooperative projects launched within ENIAC and CATRENE programmes. Mainly driven by the requirements of their IC manufacturers, they do not integrate 450mm in their support priorities, as they do not see any commitment on 450mm from indigenous IC makers and consequently any return on investment, particularly from a job creation perspective.

16.3. Return On Investment

Indeed, the return on investment from public funding is largely driven by employment creation directly at the IC maker and supplier's level but also that introduced into the entire economy through additional service creation (see Chapter 13).

The impact of advanced semiconductor manufacturing infrastructure has always proved beneficial in the past for PAs, provided a business case can be found for the corresponding infrastructure. However, in addition to the current absence of any commitment from

European IDMs to 450mm, there is also the concern that the degree of automation in state-of-the-art 450mm fabs be so high that the direct employment might be significantly reduced compared to previous wafer size generation.

From an employment creation perspective, one should note however that the traditional weight of IC makers in PAs support strategy could be offset against the fact that equipment and material suppliers represent a similar number of employees in Europe (both slightly over 100 000 direct employment in Europe). On the second hand, IC makers dominance within the supply chain is gradually decreasing as illustrated by market capitalisations of key European semiconductor companies, Figure 27.

Figure 27 – Market Capitalisation Of Major European SC Companies

Company	Market capitalisation (in billion US$)
ASML	17.3
ARM	7.8
Infineon	6.1
STM	4.9
NXP	3.9
ASMI	1.5
SOITEC	0.44

Source: Company Reports

Job creation prospects are often related to the market view, though we accept this is not always the case. In any case, the three European IDMs are no longer the dominant players they once were and indeed are now possible targets for takeovers.

Last but not least, advanced semiconductor manufacturing facilities including both IC and equipment/material production, generate very large export sales bringing a significant contribution to the balance of payments at national level. A 450mm fab would indeed generate multi-billion dollars of exports for Europe on an annual basis. The current economic situation and the national debt crisis in Europe, instead of aggravating nationalist behaviour, could thus contribute to a renewed interest for advanced semiconductor manufacturing.

Infineon Technologies purchase of the bankrupt Qimonda assets in Dresden might also be a change of heart signal towards a renewed European interest in semiconductor manufacturing. Ironically, the 2010 capacity shortages and March 11 earthquake has woken many people out of their 'wafer fabs are not strategic' complacency and reminded them losing control of wafer production means losing control of your business.

Bringing on an alternative source of supply at the drop of a hat just simply is not an option, especially given the 2-3 month minimum production cycle times, let alone any redesign and requalification issues. Due to the increased industry consolidation that it will undoubtedly trigger, the 450mm transition brings onto the table the question of the technological independence of Europe, initially in advanced CMOS but later on also for MtM technologies.

16.4. Summary & Conclusions

Europe led the 300mm transition, including equipment and process R&D via its Semiconductor 300 initiative, and could easily have done so again at the 450mm level given that many of the key 450mm technologies have been developed in Europe. Unfortunately the indigenous European semiconductor companies were not minded to so do, possibly not helped by the lack of targeted funding to consolidated the manufacturing position.

Unfortunately, during the 300mm build out in the post dot com bust era, a wave of opinion grew in Europe that manufacturing was not of strategic European importance, culminating in the bankruptcy of Qimonda due to the lack of short-term financial support. This collapse and subsequent closure robbed Europe of its most advanced high-volume fab. Prior to this, STMicroelectronics' 300mm megafab in Catania had been shelved once the fab building and utilities were completed, with the facilities now used by 3Sun (Sharp, ENEL, STMicroelectronics) for photovoltaic solar production. Both Infineon and STMicroelectonics have now stepped out of the memory business.

This lack of interest allowed CSNE at the University of Albany instead to make the required 450mm strategic investments, establishing it as the world's prime research establishment for the 450mm transition. The G450C agreement in September 2011 regrouping around CNSE the five major chip suppliers (Intel, Samsung, TSMC, IBM and Global Foundries) puts the State of New York, not Europe, in the 450mm transition driving seat for the whole semiconductor industry. The upside of this is that it should result in a more homogeneous transition compared to 300mm, with everyone collaborating effectively on a common agenda.

The European Commission's policy of funded research over many years has made Europe a world leader in technology and process development. Similarly pre-competitive applied research programmes, such as MEDEA and CATRENE, have also enabled Europe to achieve world dominant positions in semiconductor process equipment and material from ASMI, ASML, Siltronic, Soitec and others.

Where Europe has underperformed is in the field of high-volume semiconductor manufacturing, preferring to both (a) move out of advanced manufacturing to a fabless and 'fab-lite' business model and (b) exit commodity mass markets in favour of niche and speciality areas. This has led big three chip firms – STMicroelectronics, Infineon and NXP – to sell off many of their business units and become more risk adverse.

In the current climate we do not foresee any of them being willing to invest the money required to either build a 450mm fab or invest in advanced processes, but we also believe this could change in the future, inspired by the sense of a wind of change at STMicroelectonics presented by Carlo Bozotti, President & CEO, at the February 2011 SEMI Europe ISS meeting in Grenoble:

"*Professionally and personally – as the CEO of one of the world's top ten semiconductor companies, as the President of the European Semiconductor Industry Association, and as a private individual who believes passionately in what Europe has given and can continue to give to the world – I am convinced that it is both necessary and possible to have a successful and sustainable semiconductor manufacturing industry in Europe."*

It is to be hoped therefore that, given the right incentives, the 450mm transition will prove both a powerful disruptive paradigm shift (it will be) and an irresistible opportunity (it is) for STMicroelectronics and others in Europe to leapfrog their competitors into a powerful new world leadership position. This is especially opportunistic for STMicroelectronics, given their extensive breadth of technologies and world-leading expertise in real SoC, SiP and MtM solutions. Only Renesas has a comparable, but not quite as extensive, broad range portfolio of product.

Such a positive outcome for Europe is heavily dependent on the capacity to build and implement an integrated 450mm strategy leveraging resources at the national and community levels, avoiding duplication and increasing the level of coordination both within and outside Europe. An integrated 450mm strategy in Europe naturally raises many hurdles and challenges including:

- The lack of a coordinated EU industry position with regard to 450mm

  Whilst there is a necessity to support the equipment & material suppliers' transition, 450mm is not required in the foreseeable future by two of the three European IDMs (Infineon & NXP) while the third one (STMicroelectronics) will not currently commit in the short or medium term to 450mm manufacturing in Europe

- R&D labs, which are among the main assets of Europe in the global competition, also diverge on the 450mm priority level

  Their technological portfolios, partnerships and key areas of leaderships make them diverge on their perception of the time lag between MM and MtM industrial and technological bases and consequently their interest in 450mm. There is nonetheless room for improved cooperation on 450mm and discussions have already started with this objective

- Finally 450mm funding should be in parallel with any 300mm funding that is still necessary in Europe

  This will require substantial additional funding capabilities at the European and national levels in a context of budgetary restrictions

17. Scenarios & Impact Assessment

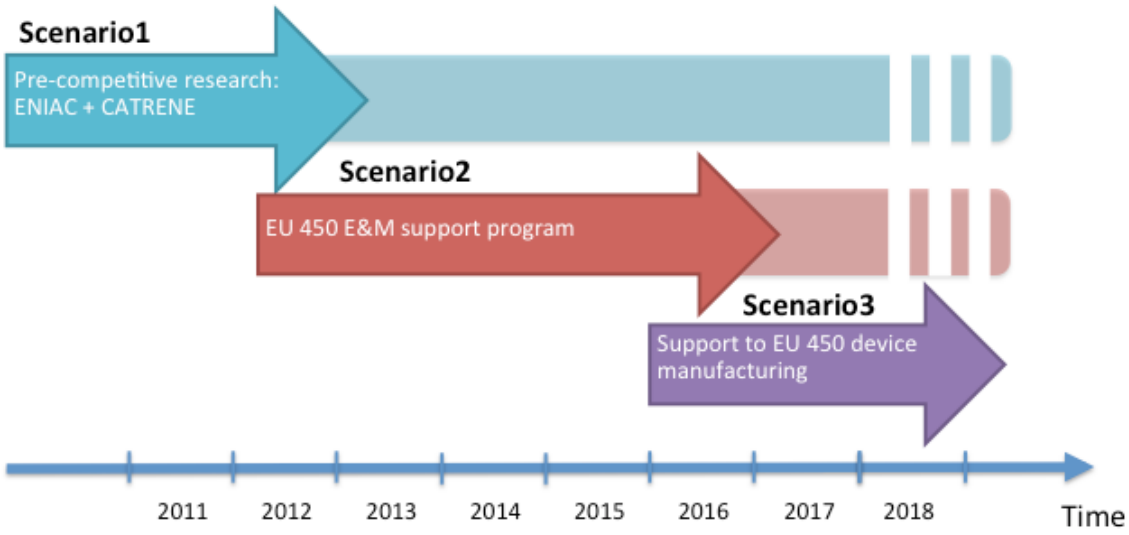
Taking into account the European 450mm context described above, the present chapter elaborates on different 450mm scenarios for Europe, their associated impact on the semiconductor supply chain, their feasibility and overall cost.

Three scenarios are being presented depending on the amount of resources available to 450mm support actions and the corresponding targets:

- Scenario 1 (business as usual): Pre-competitive research subsidies to equipment & material suppliers and R&D institutes willing to engage into 450mm cooperative development
- Scenario 2 (medium support): 450mm support programme to European equipment & material suppliers transition
- Scenario 3 (high support): Support to 450mm device manufacturing in Europe

These three scenarios correspond to a European 450mm phased approach, Figure 28, compatible with the current World and European industry positions described in previous chapters. It should be emphasized that the proposed scenarios are not mutually exclusive and that their impact for Europe is cumulative:

Figure 28 – Scenarios Phased Approach



The study team performed an impact assessment on all scenarios based on the analysis of their respective contributions to the European semiconductor supply chain and more specifically their benefits across four types of industrial activities:

- Equipment & Material design
- Equipment & Material production
- IC design
- IC production

Each impact assessment has also been segmented into different impact categories. Seven impact items have been determined and validated during the 2nd meeting of the study's Focus Group:

- **Competitiveness of EU operations**: including both manufacturing and design activities
- **Time to Market**: i.e. the capability for the EU industry to deliver competitive product sooner than competitors
- **EU attractiveness to foreign investment**: both from a design and manufacturing perspective, irrespective of the investment source (industry, wealth funds, etc.)
- **Growth in employment/revenue**: indicating the impact of scenarios on revenue and employment creation within the semiconductor supply chain (incremental growth in Europe linked to 450mm)
- **Degree of cooperation**: this corresponds to the level of cooperation between players within the supply chain induced by the implementation of the different scenarios
- **Impact on SMEs**: impact on SMEs growth and activities vary depending on the scenarios characteristics
- **EU technological independence**: this last item indicates how scenarios will contribute to secure key technological know-how and assets within Europe

Finally, impacts per item and level of the supply chain have been quantified from 1 (small impact) to 5 (large impact) based on the results of the interviews conducted as well as the study team expertise.

17.1. Scenario 1: Pre-Competitive Research Subsidies

17.1.1. Scenario 1 Description

Scenario1 is the 'business as usual' scenario, which basically consists in the support of European equipment & material suppliers 450mm R&D through pre-competitive and

cooperative programmes already in place including FP7 and coming Horizon 2020, ENIAC Joint Technology Initiative and CATRENE Eureka cluster.

Under Scenario 1, equipment & material suppliers continue to benefit from these programmes to support dedicated 450mm cooperative projects as it is currently the case with the ENIAC EEMI450, CATRENE SOI450 and NGC 450 projects with support decisions left to the Member States and the European Commission to decide on an opportunistic case-by-case basis.

It is most likely that only a very small share of the overall funding available would be dedicated to 450mm in Scenario 1 and the priority would thus be maintained on 300mm MtM development.

The following table provides a list of general Pros and Cons of Scenario 1 in the context of the global industry transition to the 450mm wafer size:

PROS
• Scenario 1 is a bottom-up approach based on European player's interest. The equipment & material suppliers would suggest and set-up projects to support their key customer requirements • All the necessary support vehicles are in place and schemes are familiar to most of the suppliers
CONS
• There would be no dedicated 450mm strategy, either at the industrial or at the member states and community levels, hence no dedicated resource allocation • EU funded projects are at the pre-competitive timescale and even CATRENE projects still entail a gap to full production

17.1.2. Impact Assessment

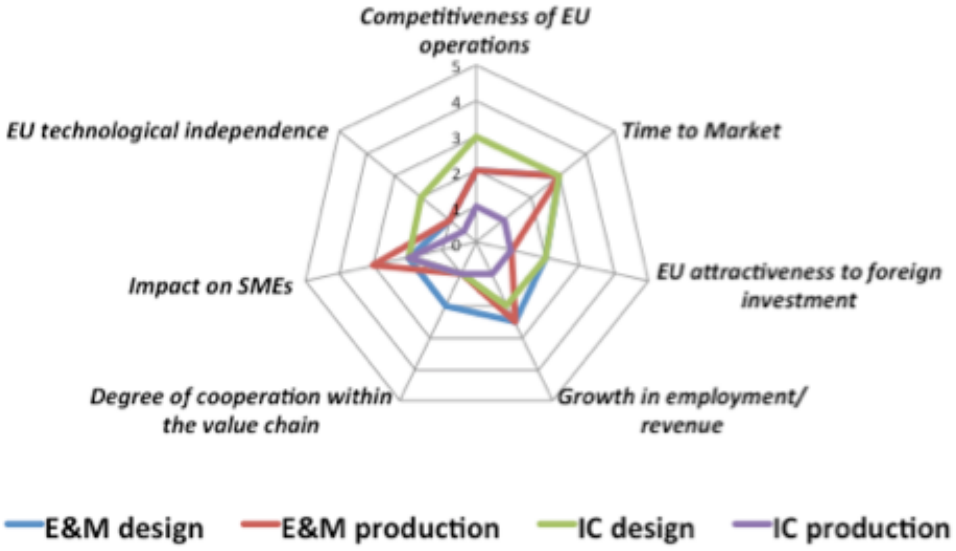
Scenario 1 has a limited positive impact on the European semiconductor supply chain which is mainly concentrated on design rather than production activities.

IC design activities are the ones expected to get the most benefit out of Scenario 1 while the smallest impact will be on IC production. Scenario 1 would reinforce the trend of the past decade and the continuous decline in semiconductor manufacturing activities in Europe.

This decline in manufacturing activities would not only touch IC production. Under Scenario1, it is indeed expected that part of equipment & material manufacturing and hence eventually R&D may move out of Europe to be nearer their customers. This is particularly emphasized by the G450C agreement in Albany with unofficial statements confirming that

companies participating in G450C will get 450mm orders and be encouraged to locate some manufacturing in the State of New York.

Figure 29 – Scenario 1 Impact Assessment



17.1.3. Cost

Scenario 1 cost estimate is based on the total funding currently available to the semiconductor industry in the different pre-competitive R&D programmes as well as an estimate of the 450mm share in this total budget.

EU framework programme for Research and Innovation

Currently funding to the semiconductor industry under the Research and Innovation framework programme corresponds to a few million euros per year and none is related to the 450mm transition.

ENIAC

Over the last four years, from 2008 to 2011, the average annual public funding to ENIAC is approximately €100 million, Figure 23 (see §15.3) although it significantly increased in 2011 when two calls were made.

Up until the fifth call held in mid-2011, only a few projects were related to the 450mm transition. The fifth call however include a significant project entitled EEMI450PR (Pilotline Readiness) building on the results from the initial EEMI450 ENIAC project, but the full details of this 5th call are not currently available.

CATRENE

Since Italy withdrew, average annual CATRENE funding by the PAs has been around €120 million in total, with France and the Netherlands the largest contributors completed by a similar amount from the companies involved, most qualifying for tax relief. Currently there are two projects related to 450mm transition: SOI450 works on SOI substrates, NGC450 deals with wafer handling. Our best case estimate is that those 450mm projects only represent 5 percent of the total annual funding within CATRENE.

To sum up, the total public funding available to European pre-competitive R&D programmes can be estimated in the range of €200 million per annum levering a similar amount of private funding i.e. a lever of roughly €400 million per annum for European cooperative R&D.

Out of this sizeable budget, 450mm projects currently represent a minor portion of the funded activities that we estimate at maximum 5 percent. We do not expect Scenario1 to bring a significant boost to 450mm funding that would most likely remain below 10 percent of the total budget available. This would naturally favour 300mm MtM R&D to the detriment of 450mm activities.

17.2. Scenario 2: 450 Support Programme To E&M Suppliers

17.2.1. Scenario 2 Description

Scenario 2 is the 'medium support' scenario, which aims at implementing dedicated support actions to accompany the European equipment and material suppliers in their transition to 450mm. The study distinguishes two different options within Scenario 2.

Option 1: 'Transatlantic bridge'

Acknowledging the global 450mm leadership of Albany, following the G450C announcement, Option 1 would consist in setting up a programme to facilitate European equipment & material suppliers' access to the G450C infrastructure for characterization and test purposes.

Such an option would basically consist in funding European equipment & material suppliers R&D projects undertaken within the framework of G450C similarly to the funding they can get in Europe for cooperative projects. Such an option could thus be based on existing cooperative research programmes but would most likely require an adaptation of the existing funding rules since most of the R&D work would be performed outside Europe.

The following table provides a list of general Pros and Cons of Scenario 2 Option 1 in the context of the global industry transition to the 450mm wafer size:

PROS
• Option 1 would enable to keep Europe in the Equipment & Material business for now since it will help maintain a link between the European industry and the most advanced development being undertaken in Albany
CONS
• However it would also eventually lead to those companies locating more of their operations, including R&D, overseas near Albany, the facility they have access to • Finally it will not leverage European equipment & material suppliers' strengths and assets in a coordinated way, hence reducing the programme efficiency and the European supply chain competitiveness

Option 2: '450E pilot line'

A second option, more ambitious, consists in creating a European 450mm equipment & material pilot line that would be based on a coordinated approach of the three major European research institutes levering their corresponding strengths in advanced semiconductor R&D (Fraunhofer, IMEC and Leti).

Due to its larger scale compared to Option 1, such a 450E "master plan" would represent a sizeable European contribution to the global 450mm transition and therefore enable a real 'negotiated' partnership and coordination with the G450C programme in Albany.

It should be noted a "pilot line" here refers to an R&D infrastructure with all the production steps available so that equipment/material/process development can take place. It is thus not the first stage of a production facility.

In the 450E programme, Fraunhofer, IMEC and Leti would agree on a coordinated working programme and the respective contribution of each institute as well. This delineation would be based on resources/skills/infrastructures of the respective institutes.

Projects being conducted within the 450E programme would be defined by material and process specialties and submitted to funding approval from the European Commission and national PAs who would decide what to support on a case-by-case basis.

The governance for such a 450E programme is a major aspect and a centralized management office structure should be created. A single industrial 'champion' tasked to lead the overall programme would directly support the centralized office while specific project leaders would be designated based on areas of expertise, reporting to the industrial 'champion' and central office.

Since it is essential that a 450E programme be opened to contributions from non-European companies, international equipment and material suppliers would be welcome to participate following the approval of a selection committee. Such participation from non-European

suppliers would also be conditioned to the payment of a fee similarly to IMEC's participation model.

Other European institutes may also join the 450E programme but the physical lab to characterize and test equipment and materials will remain in one of the three main institutes, depending on the process/material under consideration.

As soon as a formal agreement is reached on 450E between the three European institutes (ideally in Q1-2012), 450E would meet with G450C to explore and decide how both programmes could coordinate efficiently to the benefits of the entire industry.

The following table provides a list of general Pros and Cons of Scenario 2 Option 2 in the context of the global industry transition to the 450mm wafer size:

PROS
• Building on European R&D strengths, 450E would most likely keep the bulk of operations of the equipment & material suppliers within Europe and at least maintain their leadership for the long term • It would therefore reduce the investment risk for equipment & material suppliers participating in the programme and raise the level of collaboration within the supply chain both within and outside Europe • Such a programme including some degree of coordination between different locations (both within and outside Europe) would in addition represent a strong added value to develop and test 450mm wafer shipment procedures and logistic schemes
CONS
• However, such a programme is based on a significant step towards an integrated European industrial policy and requires that all the PAs and research institutes work together in a coordinated way, something neither of those groups have done well in the past • In addition, and although a 450E programme would represent a sizeable investment and impact on the transition to 450mm, we suspect it is already too late to move the 450mm centre of gravity from CSNE to Europe. Although a 450E programme would secure the current participation and involvement of world leaders in European R&D activities, it would most likely not attract any additional overseas investment and thus a significant share of the programme costs would fall on the PAs and local companies participating

17.2.2. Impact Assessment

Whatever the option being considered, the incremental impact of Scenario 2 would exclusively be concentrated on equipment & material suppliers.

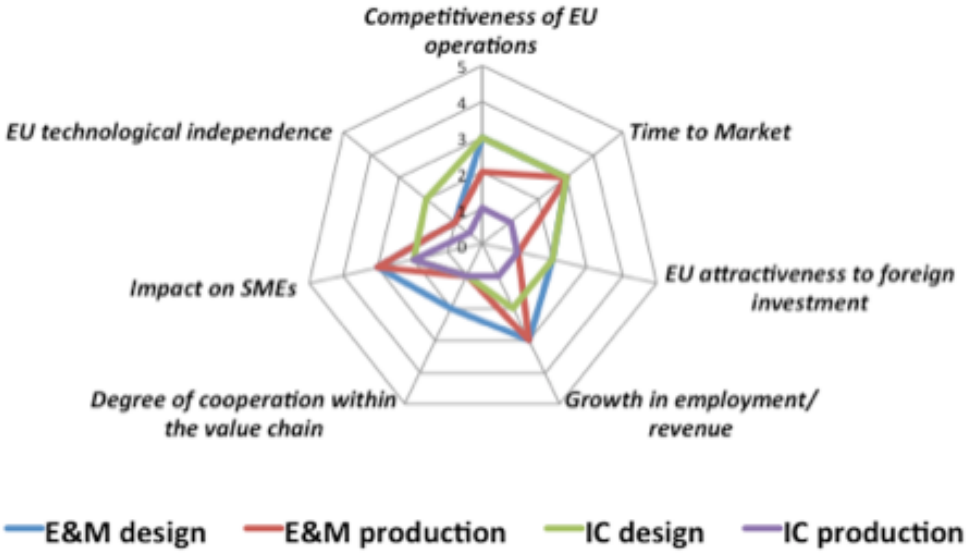
Option 1 impact: 'Transatlantic bridge'

Scenario 2 Option 1 would facilitate European equipment & material suppliers' access to State-of-the-Art 450mm R&D infrastructure and activities being performed in Albany. Its incremental benefit compared to Scenario 1 would thus mostly concern design activities.

Positive impacts are expected on the competitiveness of EU operations, the growth of employment and revenue (driven by increased activity abroad) and finally SMEs who may benefit from such a programme to take a risk they would not have taken otherwise.

Impact on the equipment & materials design activities, although limited in scale, might in turn generate some small and short-term benefits in terms of European equipment & material production.

Figure 30 – Scenario 2 (Option 1) Impact Assessment



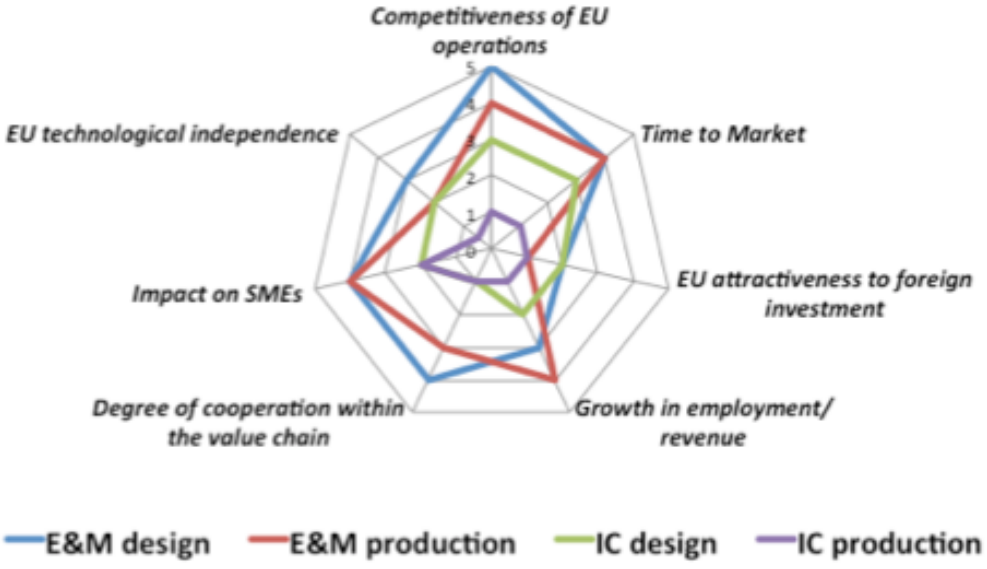
Option 2 impact: '450E pilot line'

Thanks to the coordinated move of leading research institutes, a 450E pilot line in Europe would take advantage of the global 450mm transition to consolidate the European equipment & material leaderships and hence strengthen the SC supply chain in Europe.

450E incremental impacts would indeed cover a larger number of items with balanced benefits between design and production activities for equipment & material suppliers. The overall competitiveness of EU operations, the time to market as well as the degree of cooperation within the supply chain would be significantly improved. 450E would further encourage the involvement of SMEs in the 450mm by reducing the entry barriers compared to the G450C initiative.

As already mentioned, it should however be emphasized that the G450C has already taken the leadership in the transition to 450mm and it is therefore not expected that a 450E pilot line would attract significant additional foreign investment in Europe. Nonetheless one should take into account that such a programme would definitely secure the current involvement of key semiconductor market leaders in European R&D that could be otherwise tempted to move out of Europe.

Figure 31 – Scenario 2 (Option 2) Impact Assessment



17.2.3. Cost & Feasibility

The study team provides hereafter a 450E master plan cost estimate based on the following key consolidated hypotheses:

- Cost of 450mm transition, representing the total investment required to bring production-ready 450mm tools and materials on the market:

  - 5000 people per annum over 5 years

- Number of people working in the G450C clean room facility in Albany:

  - 400 people dedicated to 450mm development

- Cost of 450mm transition, representing the total investment required (Cap Ex[2]+Op Ex[3]) to bring production-ready 450mm tools and materials on the market:

  - B**etween US$25 billion and US$40 billion depending on sources**

[2] Capital Expenditure
[3] Operation Expenditure

Applying to these fundamental hypotheses some cost structures derived from the study team internal expertise [4], we extrapolated the total cost of the 450mm transition at the World and European levels, including the cost of shared technological research facilities similar to G450C in Albany or 450E in Europe.

The following results correspond to the total cost of a five-year program from 2012 to 2016 enabling the development of production-ready equipment and materials including both Capital and Operating Expenses:

- World = US$37 billion, including G450C @ US$3 billion
- Europe = US$7.5 billion, including 450E @ US$1.5 billion

It is most likely that PAs would never fund Cap Ex costs outside Europe under Option 1 and therefore eligible cost would be restricted to Op Ex costs i.e. US$500 million over the programme period.

In Option 2 however, it is instead likely that both Op Ex and Cap Ex would be eligible since they would be incurred inside Europe i.e. US$1.5 billion over the program period.

Applying a 50 percent funding ratio to these estimates which is the accepted rule in European cooperative R&D programmes provides the following public funding requirement for Scenario 2 options:

- Option1 cost = US$250 million over 5 years i.e. approximately **20 percent of current budget** available for European pre-competitive R&D in the semiconductor industry
- Option 2 cost = US$740 million over 5 years i.e. approximately **55 percent of current budget** available for European pre-competitive R&D in the semiconductor industry

Whereas the 'Transatlantic bridge' (Option 1) could be envisaged in current budgetary conditions and provided that the 450mm share be increased in current programmes, it is not possible to implement the '450E pilot line' option without a massive limitation of current 300mm and MtM funded R&D.

Since both 300mm and 450mm R&D activities should be undertaken in parallel, implementing the 450E programme requires that current funding available for the semiconductor industry be significantly expanded. This could only be envisaged if all funding sources available at European and National levels are leveraged, which is in favour of a 450E decentralised infrastructure based on working areas delineation (but with centralised programme management).

[4] Calculation based on the following key hypotheses:
- European equipment & material world market share = 20%;
- Opex basis: €250k (salary + taxes), additional expenses/consumables = 1/3 of total Opex per employee;
- Euro/dollar conversion = 1.32

17.3. Scenario 3: Support To 450mm Device Manufacturing In Europe

17.3.1. Scenario 3 Description

Scenario 3 is the 'high support' scenario, which would enable 450mm device manufacturing in Europe by the end of the decade thanks to appropriate support framework conditions and provided the existence of an industrial commitment. Similarly to Scenario 2, the study team identified three distinct options in Scenario 3, depending on the 450mm fab typology and business model.

Option 1: 'Private 450mm fab'

Considering the current state of European IDMs, it is not realistic to envisage that one of them would solely invest in a 450mm fab before 2020. A private 450mm fab option in Europe would therefore correspond to the commitment and investment by a non-European company. There are currently only two potential candidates for such an investment, namely Intel and Samsung.

The following table provides a list of general Pros and Cons of Scenario 3 Option 1 in the context of the global industry transition to the 450mm wafer size:

PROS
• A private 450mm fab would maintain advanced node and MM device manufacturing in Europe
CONS
• Such a private fab would most likely be a copy of an existing 450 fab with consequently reduced externalities and links with the European semiconductor ecosystem • Access to EC financial support might also be more difficult

Option 2: '450mm foundry'

Similarly to Option 1, there are only two potential candidates for a 450mm foundry investment in Europe: Global Foundries and TSMC.

The following table provides a list of general Pros and Cons of Scenario 3 Option2 in the context of the global industry transition to the 450mm wafer size:

PROS
• A 450mm foundry would stimulate close contact with the fabless and European design IP community, attracting design resources and generating more products • This would also favour the links with the European research institutes and facilitate the access to EC financial supports
CONS
• The infrastructure to fully support a 450mm fab must be developed. It is expected to be more expensive than in the case of a private fab since foundries are not copycats of existing facilities

Option 3: '450mm consortium'

Finally, the 450mm consortium option corresponds to a shared fab model where several IC makers jointly invest into a 450mm fab in Europe. Such a consortium would be part of a European plan to support a global platform performing device, material and equipment R&D as well as production.

A 450mm consortium is not seriously envisaged at the present time since there is no commitment from any European indigenous IDMs either on 450mm or a shared manufacturing strategy, despite the fact the study team feels this is the right way to go.

It should not be ruled out though since the 450mm wafer scale up will profoundly change the manufacturing landscape by the end of the decade and could thus lead to new forms of business models or partnerships. This industry bifurcation will undoubtedly impact IC makers, equipment & material suppliers and national strategies as well.

Two approaches could be envisaged to Option 3 depending on the consortium potential participants:

- **450mm MM fab** – dedicated from the early start to the most advanced nodes. This approach would replicate the Crolles Alliance on 450mm with a larger scale facility in order to be competitive. Such a MM consortia would involve at least one foundry partner

- **Eurofab450** joint venture focusing on MtM volume products at the beginning, i.e. probably at the 65nm node and above, but capable to be upgraded to process MM technologies in due time. Although not envisaged currently by the industry since not in the plans of the early 450 adopters, we believe that using 450mm wafer to produce advanced MtM products on more mature nodes is not only a decent possibility but would have many merits for Europe and should at least be debated. Such a consortium could be envisaged as a joint venture between European or foreign IDMs.

The following table provides a list of general Pros and Cons of Scenario 3 Option 3 in the context of the global industry transition to the 450mm wafer size:

PROS
• A joint fab in Europe would be part of a global plan to support an advanced manufacturing platform in Europe including device, material and equipment R&D • This would strongly encourage industrial cooperation within Europe and links with the European institutes, strengthening Europe semiconductor supply chain • A European consortium would finally facilitate access to EC financial supports
CONS
• Industrial commitment is missing and no interest expressed by any actor yet • Sharing manufacturing assets with direct/indirect competitors has not proved to be successful in the past and creates some risks and difficulties

17.3.2. Impact Assessment

Whatever option is considered in Scenario 3, a European 450mm fab would bring some generic benefits to Europe:

- First an admittedly large subsidy in state-of-the-art semiconductor manufacturing leverages a very large inward investment and Return On Investment for PAs as already proven in the past
- Among these benefits is the fact that advanced manufacturing facilities are very strong contributors to the balance of payments generating multi-billion dollars exports sales every year
- Upstream in the supply chain, European suppliers would also gain local access to a fab capable of qualification for future production equipment and materials
- A European 450mm fab would thus maintain advanced manufacturing knowledge and secures a comprehensive semiconductor supply chain in Europe, securing its technological independence in advanced semiconductor processes and products and its capability to seize new market opportunities in the future
- This would finally strongly contribute to focus educational establishments back onto the semiconductor industry, answering the brain drain dilemma faced by Europe

Despite the above-mentioned benefits, the establishment of a 450mm fab raises severe hurdles in Europe including:

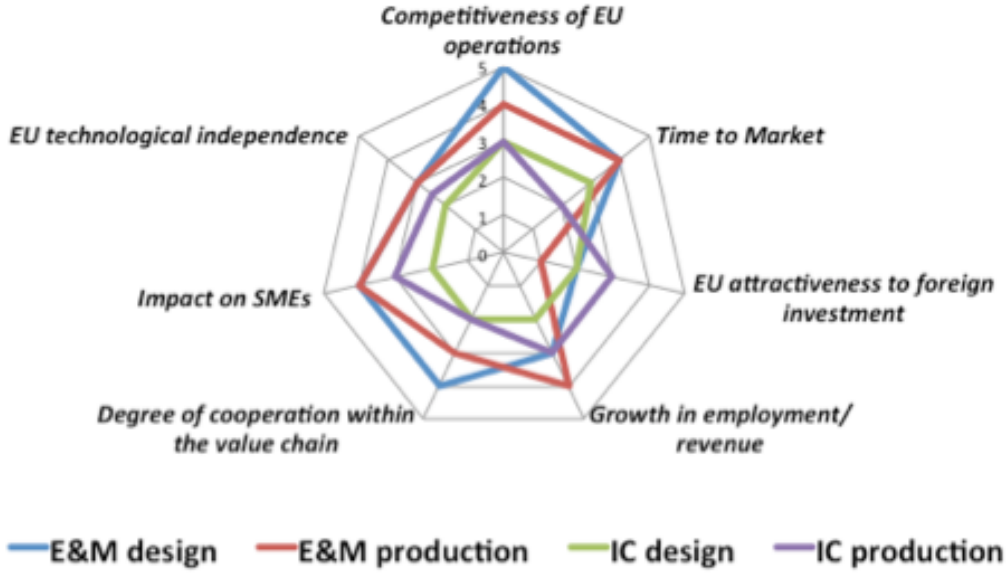
- There is currently no industrial commitment to 450mm in Europe and incumbent players resources are not large enough for such an investment anyway
- The infrastructure to fully support a 450 fab in Europe must be developed and would certainly add to the overall investment
- Contrary to the 450E programme (Scenario 2 Option 2), a 450mm fab will be located in a unique place. Although it is reasonable to think that the impact of such an investment will be felt across Europe, this will most likely generate difficulties to aggregate all funding levers

Option 1 impact: Private 450mm fab

A private 450mm fab in Europe would most likely be the copycat of an existing 450 fab. Such an investment in Europe would be used to extend the production capabilities of an inward investor with no major influence on the location of the design centres. The impact of a private 450mm fab in Europe would thus be almost exclusively focused on IC production activities with only very limited impact on IC design and equipment & material activities in Europe.

Major incremental impact would be felt on the competitiveness of EU operations, the attractiveness to foreign investment and the overall growth in employment/revenue in IC production. Due to the relative lack of openness of such a fab, the technological independence of Europe as well as the degree of cooperation within the supply chain would be less impacted.

Figure 32 – Scenario 3 (Option 1) Impact Assessment



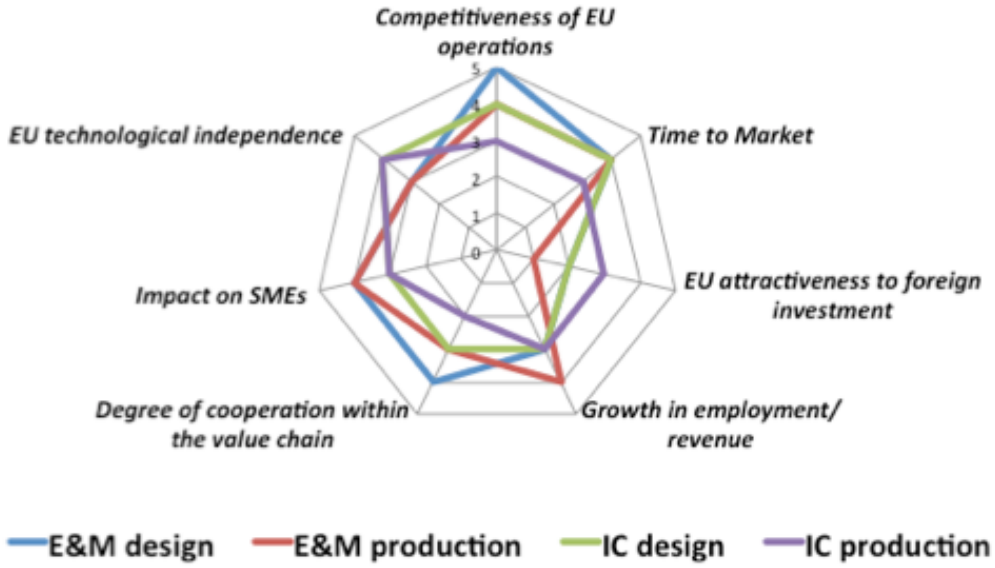
Option 2 impact: 450mm foundry

Contrary to the 450mm private fab, it is expected that a 450mm foundry in Europe would also have a significant impact on IC design activities in Europe. A 450mm foundry would stimulate close contact with the fabless and European design IP community, attracting design resources and generating more products.

All impact items would be favourably impacted with the notable exception of the EU attractiveness to foreign investment. Indeed we do not expect that the presence of a 450mm foundry in Europe would contribute to increase inward investment in IC design activities in Europe but will rather build on existing capabilities, secure and develop European strengths in this domain.

A 450mm foundry in Europe would also have a positive and incremental impact on IC production activities, strengthening the Time to Market and EU technological independence.

Figure 33 – Scenario 3 (Option 2) Impact Assessment



Option 3 impact: 450mm Consortium

Finally, a 450mm shared-fab is seen as the ultimate solution maximizing the benefits for all supply chain activities in Europe. The impact of such a 450mm consortium in Europe would slightly vary whether the fab will focus on MM or MtM products.

It is expected a Eurofab450 focusing at the start-up on MtM products will generate the largest benefits in Europe due to a better fit with current European IDMs portfolio and an agile and evolutionary approach to the 450mm transition. This infrastructure could greatly and rapidly strengthen the competitive position of involved European IDMs to the benefit of the whole

European semiconductor supply chain while providing a gateway to MM advanced technologies when required.

Whatever the Option 3 approach is, a 450mm shared-fab would further contribute to the degree of cooperation within the supply chain, the competitiveness of EU operations (IC only), the time to market, the technological independence of Europe and the attractiveness to foreign investment (equipment & material only).

Figure 34 – Scenario 3 (Option 3) Impact Assessment – MM fab

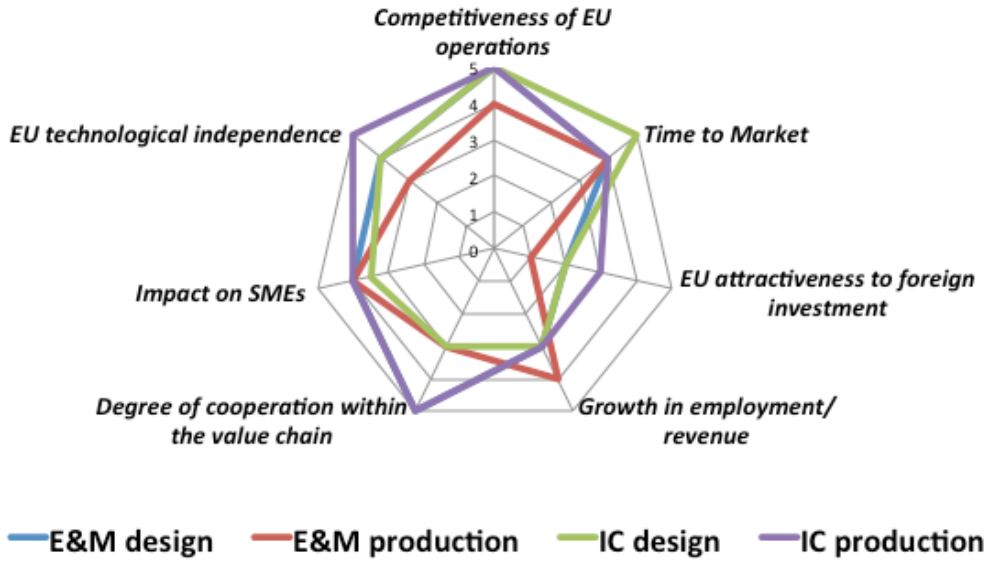
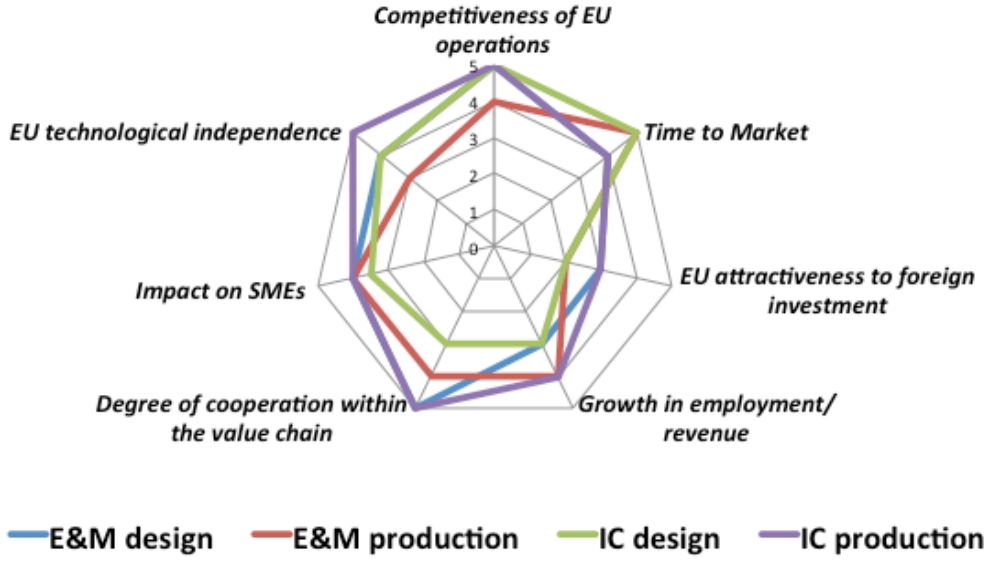


Figure 35 – Scenario 3 (Option 3) Impact Assessment – Eurofab450



17.3.3. Cost

Building on the expertise of the study team, we have attempted in this Report to delineate the cost structure of a Eurofab 450 programme originally focused on MtM production at 65nm and above, but capable in due time to process advanced nodes down the ITRS roadmap, Figure 36. Such a cost estimate has been elaborated based on 300mm known cost structures and current 450mm estimates with the following baseline hypothesis:

- Location: Greenfield site in Europe
- Output: 8k wafers/week natural wafers (300mm or 450mm)
- MtM configuration: 90nm to 60nm processing
- MM configuration: up to 28/22nm processing

Figure 36 – Cost Of 300mm vs. 450mm MtM & MM Fabs

	300mm More than Moore	300mm More Moore	450mm More than Moore	450mm More Moore		450mm More Moore
Node (nm)	90/60	28/22	90/60	28/22		20/15/10
Photolithography	No immersion	Immersion	No immersion	Immersion		Immersion
Clear Room size (in sq ft)	18,300	21,300	24,000	32,000		40,000
EUV Capex cell (1k wow)	No	Yes	No	Yes		Yes
Capex total for tools + hook up (full capacity)	78%	88% (with EUV)	79%	86% (with EUV)		85% (with EUV)
Including Photolitho, Metrology, Defectivity	48%	53%	50%	60%		60%
Including Building/Facilities/Automation	22%	12%	21%	14%		15%
GRAND TOTAL (in billion $)	**3.4**	**7.7**	**4.7**	**10**		**14**

Source: Laurent Bosson

It should be emphasized here that the above-mentioned wafer output characteristics only correspond to the first step of a European 450mm fab. Any 450mm production fab in Europe must be designed to be converted into a high-volume state-of-the-art fab, competitive with anything e.g. TSMC might construct, but initially only constructed and equipped with the equipment and facilities needed for lower technology node and production volumes.

What this table shows is that, for any given technology node, the 30 percent to 38 percent additional cost of a 450mm fab compared to an equivalent 300mm fab will be clearly outweighed by the 2.25 times increase in wafer fab output.

We acknowledge that this step-by-step modular approach inevitably involves a cost penalty compared to massive up-front investments in the equivalent high-volume MM fab, but the massive added value benefits make this modest penalty easily affordable.

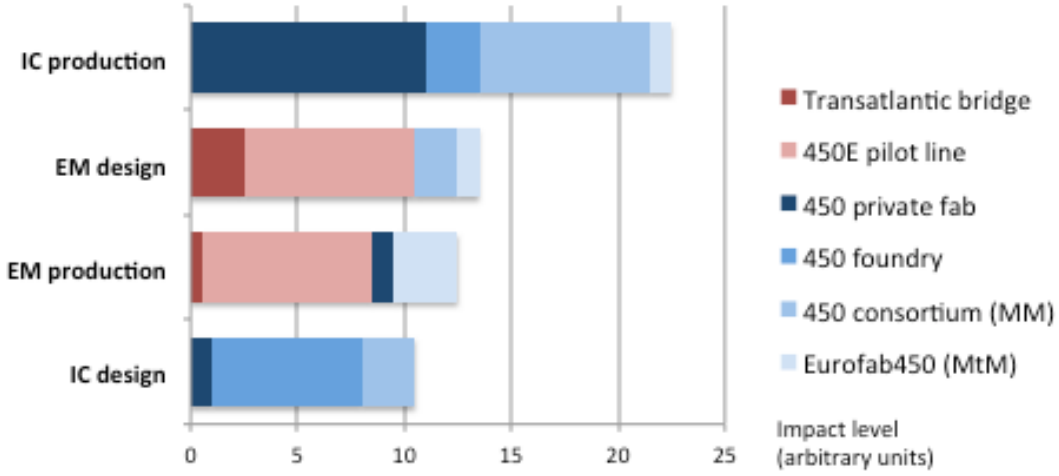
An extrapolation has also been made in Figure 36 as to the likely cost of a '20/15/10nm capable' 450mm fab with similar wafer output based on Industry expectations for the 20/15nm process and our early assumptions for 10nm, although there are obviously still lots of uncertainties on the process characteristics and associated costs.

Depending on the configuration, a 450mm fab in Europe would thus require total subsidies in the range of US$1 billion to US$3 billion including both up-front subsidies and on-going incentives cumulated over the life of the fab (up to 10 years), towards a total fab cost of US$4.7 billion to US$10 billion respectively.

17.4. Cumulated Impact Of Scenarios

As indicated in Figure 37, the cumulative impact of scenarios and their associated options primarily concerns IC production followed by equipment & material activities (design and production) and finally IC design.

Figure 37 – Cumulative Impact Of Scenarios (Per Type Of Activity)



The 450E pilot line demonstrates by far the largest impact on the European equipment & material supply chain with strong benefits on both design and production activities.

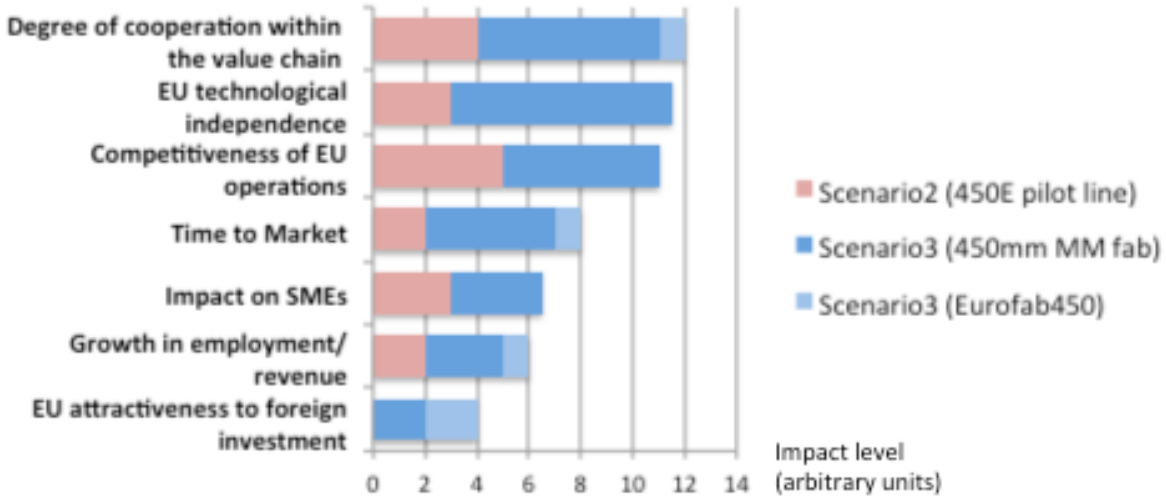
A 450mm fab in Europe would benefit to both IC and equipment & material activities and thus generate a larger impact on the entire semiconductor supply chain although this needs to be analysed depending on the fab profile:

- 450mm private fab would mostly benefit to IC production activities

- 450mm foundry fab would incrementally benefit to IC design activities
- 450mm MM consortium would represent a further boost to IC production and design activities
- Compared to a MM consortium a Eurofab450 focused on MtM products would provide an extra benefit to equipment & material design/production and IC production activities as well

Figure 38 indicates the maximum contribution of both scenarios per impact item.

Figure 38 – Cumulative impact Of Scenarios (Per Type Of Impact)



Impact items can be classified into three main categories depending on the importance of the scenario contribution: large, medium or small impact.

Largest scenarios impacts are concentrated on the degree of cooperation within the European value chain, the technological independence of Europe and the competitiveness of operations in Europe. In other words, scenarios will build on existing European strengths and secure the advanced semiconductor industrial base in Europe, which would otherwise be threatened by the 450mm transition.

Scenarios will give medium benefits on the time to market, SMEs and the overall growth in employment and revenue for Europe. Indeed it is expected that Albany will define the 450mm transition timeline and only few entrants will penetrate the market in 450mm with the exception of specific fields like metrology requiring new concepts and tools.

Finally scenarios do not anticipate any significant change in the European attractiveness to foreign investment since it is not expected that the centre of gravity can be moved out of Albany following the G450C agreement.

One should however not underestimate the influence of scenarios on employment and attractiveness to foreign investment. The main outcome of scenarios is indeed to secure the existing European strengths and industrial base and it is a decent possibility that without their implementation, the semiconductor employment in Europe will decrease (in particular equipment & material suppliers) and foreign investment in Europe will diminish (in particular in advanced R&D activities).

17.5. Conclusions On Scenarios

Europe will not secure its long-term position in advanced semiconductor manufacturing without defining and implementing a coordinated 450mm strategy. This should not however be to the detriment of the parallel 300mm investment needed by European chip firms for the development of future integrated systems.

Given the various possible scenarios, an ideal integrated approach towards a real 450mm European strategy can be summarised as follows:

Phase 1: 2012 to 2017

- **Objective:** Support equipment and material suppliers transition to 450mm (1st priority)
- **Output:** Basic research complementary to G450C activities and pre-production tools for European equipment suppliers leveraging the strength of existing European cooperation network
- **Instruments:** Combination of existing cooperative R&D programmes (Scenario 1) and 450E pilot line (Scenario 2 Option 2)
- **Cost (public funding):** Over half of the current budget for SC cooperative R&D in Europe over the next five year (US$150 million per year)
- **Funding mechanism:** Existing instruments (ENIAC/CATRENE) with an increased contribution by EC together with new forms of funding and rules (see KET Report: pilot line funding) in order to increase the total budget to such levels that it will be possible to perform both 300mm necessary development and 450mm investment in parallel

Phase 2: 2016 to 2020

- **Objective:** Support the development of 450mm production facility(ies)
- **Output:** This depends on the fab typology (MM vs. MtM) but will either maintain and/or secure long-term European leadership and access to the most advanced SC

technologies. To ensure an integrated approach, Phase 2 needs to be undertaken in a timely manner to provide an industrial environment for the equipment/material suppliers to follow-up on their investments made in Phase 1

- **Instruments:** Grants, tax concessions, special loans and infrastructure investments, etc. In the case of a joint fab structure this could also be based on some kind of European-level funding

- **Cost (public funding):** Total subsidies in the range of US$1 billion to US$3 billion depending on the fab configuration including both up-front subsidies and on-going incentives cumulated over the life of the fab (up to 10 years). This requires **s**etting the right investment framework to favour Foreign Direct Investment in state-of-the-art MM 450mm at national level and/or defining a common European strategy between EC and the parties involved for the development of a MtM 450mm joint fab

Phase 3: 2020 & beyond

- **Objective:** Continue to ensure attractiveness of Europe to SC manufacturing investment

- **Output:** Support a pilot line for the post-CMOS era and start the next innovation cycle. In a truly integrated approach this would ideally utilise the previously developed 450E infrastructure

- **Instruments:** On-going 'maintenance' support for the EU-based 450mm infrastructure together with similar Phase 1 instruments to develop the post-CMOS technology and associated equipment and materials

- **Cost:** Similar in relative size to Phase 1 for 450mm; prohibitive, if even do-able, without the successful implementation of Phase 1 and Phase 2 given that by 2020 450mm will be the only viable platform for advanced SC development

Such a European long-term vision and strategy would thus be phased, gradual (as far as the investment is concerned) and inclusive (upstream and downstream investment) ensuring a virtuous cycle in Europe which is completely aligned with the KET Report recommendations.

Europe is currently leading the world in MtM technologies but this leadership is at risk being dependent on an indigenous semiconductor production platform that is predominantly 200mm and smaller wafer-size based. This is not currently a major disadvantage but by 2020 it will be once 300mm MM production migrates to 450mm technology pushing a sizeable part of today's 300mm MM production to MtM, as is anticipated.

As such, the integrated approach outlined above represents an ideal European opportunity, not only to maintain its current 'MtM' world lead but to also enable it to re-enter the 'MM' manufacturing opportunity, a key part of the KET strategic vision. It is an innovative approach to the 450mm transition based on European strengths in R&D, market and cooperative development.

For Europe's indigenous chip firms, entering 450mm on MtM would immediately marginalising all of its 150/200mm and prospective 300mm competitors in a stroke, whilst at the same time progressively introducing MM technologies, initially with the low volume products currently processed internally.

The 450mm line could be run as an independent co-operative 'foundry' but with ownership by the IDM partners; it could also offer foundry services as part of the Europractice programme to support Europe's fabless semiconductor community.

It could also eventually offer broader foundry services to the large fabless firms such as Broadcom, Qualcomm, nVidia and others. Industrial partners need not be confined to just Europe's indigenous chip firms but could also include other firms abroad, for example Freescale and Renesas, each committing to purchase a proportion of the capacity in proportion to their share of the total investment cost.

The precise investment and operating details would obviously need to be worked out but conceptually the plan is workable; it is after all the same model as buying from an external foundry except now the foundry customers are also the owners. Run properly, this would not only allow Europe to leapfrog to the forefront of chip manufacturing technology overnight, it also offers potentially a greater security of supply and lower cost. It would also provide a vital home base for Europe's equipment and materials industry and advanced research centres, a real win-win scenario all round.

Appendix 1 – Glossary Of Terms

Term	Definition
ALD	Atomic Layer Deposition (advanced deposition process)
APC	Advanced Process Control
ASP	Average Selling Price
CAM	Computer Aided Manufacturing System
CDMA	Code Division Multiple Access – refers to the US mobile communication standard
CMOS (Post-)	Complementary Metal-Oxide Semiconductor is the dominant technology for constructing integrated circuits. Post-CMOS refers to the expected transition to new forms of integrated circuits based on carbon structures, etc. which are expected to develop below the 5nm/8nm node
CMP	Chemical Mechanical Planarization – used to smooth the surface of a Silicon wafer with the combination of chemical and mechanical forces
CVD PVD ALD	Chemical Vapor Deposition – Plasma Vapor Deposition – Atomic Layer Deposition (advanced deposition techniques used in the semiconductor manufacturing process)
Die	Refers to the chip itself. Hundreds of dies are being processed in parallel on the same semiconductor wafer
DRAM	Dynamic Random Access Memory
E-beam	Electron- beam lithography – refers to one of the next generation lithography technologies possible under development for advanced technology nodes (also called mask-less lithography)
EDA	Electronic Design Automation – software used in the semiconductor design flow
EEMI450	European 450mm Equipment & Materials Initiative
ESIA	European Semiconductor Industry Association
EUV	Extreme Ultra Violet – refers to one of the next generation lithography technologies that will be eventually necessary to produce chips below 22nm
FinFET	Fin-based multigate transistors architectures used at the most advanced technological nodes (e.g. Intel's Tri-Gate transistors)
FOSB	Front Opening Shipping Box – used to ship processed wafers to other location (back-end facilities)
FOUP	Front Opening Universal Pod – used to convey wafers throughout the different process steps within the fab
G450C	Global 450 Consortium – based in Albany (New York State) and regrouping Intel, TSMC, Samsung, IBM and Global Foundries in order to speed-up and coordinate the development of 450mm equipment and materials
GDP	Growth Domestic Product
GDS-II	Database file format which is the industry standard for data exchange of integrated circuit or IC layout artwork

Term	Definition
Giga-Fab	Refers to TSMC's concept of duplicating and interconnecting fab modules to create very large manufacturing infrastructure with capacities above 100k wafers per month (native wafers)
Hi-k metal gate (HKMG)	Refers to materials used in advanced transistor designs in order to improve transistor performance (leakage and reliability)
IC	Integrated Circuit
IDMs	Integrated Device Manufacturers with both design and manufacturing capabilities (as opposed to fabless and foundries pure-play business models)
IP	Intellectual Property
ISMI	International Sematech Manufacturing Initiative
ITRS	International Technology Roadmap for Semiconductors
KET	Key Enabling Technology
MCU/MPU	Microcontrollert / Microprocessor
MEMs	Micro-ElectroMechanical systems – refers to speciality manufacturing processes enabling the use of silicon or other semiconductor substrates to design micro-sensors, actuators, etc. and possibly integrate signal processing/control/interface onto the same chip
MES	Manufacturing Execution System – software used to optimize and control the manufacturing operations within a semiconductor plant
MM	More Moore – referring to the most advanced (miniaturized) SC manufacturing processes, currently below 65nm
MtM	More than Moore – referring to complementary integration techniques and SC processes like sensors, analog, heterogeneous modules (System in Package), etc.
Nano-imprint	Nanoimprint lithography (NIL) is a patterning method in which a surface pattern of a stamp is replicated into a material by mechanical contact and three dimensional material displacement
OEM	Original Equipment Manufacturer
PA	Public Authority
PV	Photo-Voltaic
SC	Semiconductor
SiGe	Silicon-Germanium – other base material for semiconductor wafers with improved performances compared to Silicon albeit higher cost
SiP	System in Package – refers to the integration of different chips in a single package in order to provide a complete system
SoC	System on Chip – refers to the integration of different elements of a functional system into a single silicon chip (e.g. memory + processors + wireless interfaces etc.)
SOI	Silicon On Insulator – refers to a specific substrate manufacturing techniques providing higher transistor performance and lower energy consumption compared to bulk Silicon wafers (at identical transistor design)

Term	Definition
SRAM	Static Random Access Memory
TSV	Through Silicon Via – technology used to interconnect several dies vertically (3D modules).
UTB (FD-SOI)	Ultra Thin Body (Fully Depleted Silicon On Insulator) – refers to a competing transistor architecture to FinFET based on SOI wafers
wpm	Wafer out per month – refer to the output capacity of a semiconductor wafer fab (front-end)

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Appendix 2 – Interview Guide

This document is intended to guide interviewers through the industry interviews for the EC funded project SMART 2010/062 in order to ensure we obtain the information necessary for the final Report.

Introduction

We have made the fundamental assertion that 450mm wafer manufacturing will now take place. It had been delayed for several years but recently three companies (Intel, TSMC and Samsung) have all now asserted that they will begin production using these wafers in newly equipped fabs at around the mid-point of this decade.

It is thus not for us to discuss 'if' 450mm wafer production should happen but 'what the level of European participation in its implementation should be'. The questions have thus been divided up into several areas, not all of which will be applicable to all respondents.

NB: Four types of semiconductor manufacturing infrastructures are considered in this document with the following definition:

- *Technological research facility used to develop key manufacturing stages/technologies but which does not have the complete/balanced equipment set (i.e. not a full production line), also referred to as 'integration line' (e.g. Leti, IMEC and Albany)*
- *Pilot lines for technology node / product demonstration with two different profiles*
  - *Pilot line with limited room for subsequent expansion such as Crolles*
  - *Pilot line that is intended for expansion to a high volume fab, for example Intel's D1X or TSMC's fab 12*
- *High-volume manufacturing facility, as is typical for foundries, memories and Intel fabs*

Semiconductor Manufacturing

First we ask some general questions to get things moving. Obviously if the interviewer knows the interviewee this may be unnecessary.

Q1. What do you see as Europe's main strengths in the semiconductor market? Unfortunately the European share of the market has declined in recent years but do you believe that with the appropriate nurturing a full recovery can be made and Europe regain the position it once held?

Q2. Are you active in the 450mm wafer working groups and do you find them effective? What is your current thinking about 450mm wafers in general and more specifically for your company? If positive, what are the major reasons you support a transition to 450mm?

Q3. Do you see any opportunity for Europe with respect to 450mm development? What could be the benefits of such a transition?

Early 450mm Fabs & Products

Next we wish to deal with the initial market for 450mm wafer fabbed products.

Q4. Do you think the transition to 450mm wafers is dependant or independent from the introduction of a given technology node? Also do you see it driven by a certain die size or do you think it will be die size independent?

Q5. Do you think the introduction of 450mm could lead to a "2-speed" semiconductor industry with 450mm deployed only for very high volume and "mono-product" manufacturing?

Q6. Do you think that 450mm will be “dedicated” only to advanced process, or do you think that it could also made viable for more mature processes as is happening today for 300mm analogue or 200mm and possibly 300mm for MEMS?

Q7. It is reasonable to assume that Intel’s first product built on 450mm wafers at their D1X fab will be their latest processor. The latest predictions are for the first 450mm pilot production line to be operational in 2015 and, after ramp-up using the 16nm process, will target the 11/12nm node. Do you believe this is realistic? Note this is purely from a planning and build perspective. Please leave discussions on the technological risks that could cause delays until the section on this.

Q8. (IDMs and fabless) When do you believe you will first have a product fabbed on a 450mm line (in your own fab or foundry produced) and for what application area is it likely to address? With what technology node will you start 450mm?

Q9. What advantages do you anticipate 450mm wafers initially offering you, if any – a technology only available on 450mm, or primarily cost benefits? If cost benefits what will most likely be the main driver behind those benefits?

Q10. Do you see a risk of a world-wide capacity shortage due to the lack of new 300mm fabs being constructed while we wait for the 450mm introduction?

450mm Manufacturing/Business Models & Conditions

We now wish to discuss how the EC could encourage semiconductor manufacturing in Europe at the 450mm wafer size. We will discuss possible improvements to European 300mm wafer capacity separately in a later section.

Q11. What is the optimal manufacturing landscape you have in mind for SC in Europe? What is your cost estimate for achieving this and what would be the benefits?

Q12. Statements are often made within Europe that the semiconductor industry is not a level playing field. The problem is that we often hear similar statements made in Japan, the US and even in places in the Far East such as Singapore. We would therefore be most grateful to receive any particular facts and evidences of regional framework distortions you may be able to send us regarding R&D activities, IC manufacturing and also Equipment & Material supply. Please be assured that all information will be treated in the strictest confidence.

Q13. Could you elaborate on the benefits and impacts that 450mm manufacturing in Europe (and conversely the lack of 450mm in Europe) would have across the value chain:

- R&D?
- Equipment and material suppliers?
- IC design and manufacturing?
- End-user industries such as automotive, consumer, telecom and healthcare?

Q14. What kind of cooperation or partnership would you propose to support the creation of a 450mm fab in Europe? Please differentiate between a technological research facility, a pilot line for technology node / product demonstration and a volume manufacturing facility?

Q15. Under what condition would your company launch or participate to such a fab in Europe (technological research, pilot line, volume manufacturing)?

Q16. Alternatively do you believe the EC and governments should not make any such financial support for a 450mm fab? If so are there other activities they should support to encourage advanced semiconductor manufacturing within Europe?

Q17. What do you believe is the minimum viable size, in wafers per month, for a European based 450mm fab? Please differentiate your answer between a pilot line vs. a volume manufacturing fab? Please also state if using the number of 450mm wafers or the 200mm wafer equivalents (one 450mm wafer = five 200mm wafers)

Q18. (IC manufacturers) Do you anticipate your model of your own 200mm/300mm fab together with your current external foundries being suitable for your needs over the next decade or would you be interested in business with a European based 450mm wafer fab if it was suitably qualified?

Q19. Does the increased number of die per wafer generate new needs regarding wafers lot management? And of lot size? Would you think that this lot size effect will drive new concepts about wafer fab organization and layout? Assuming your company would benefit from a conversion to 450mm, would you support a different standard "lot size" compared to the current one anticipated, i.e. less than 25 wafers? Do you see a need for new process control strategy linked to a reduced number of wafers per process within a given time?

Effect Of 450mm On 300mm Manufacturing Models

Now we wish to discuss the effect that 450mm will have on 300mm manufacturing models. We need to consider the risk that future new technologies will only be developed for 450mm and also ascertain the future of these fabs once 450mm fabs are well established worldwide.

These questions are for fab companies and their equipment suppliers.

Q20. At the 200mm/300mm transition, development of improved 200mm equipment ceased and so all future advanced technologies were forced to utilise 300mm wafers with only minimal improvements made to 200mm process equipment thereafter. Do you think the

300mm tool generation will continue to be developed and available to support the ITRS roadmap and all the technology nodes forecasted along the roadmap?

Q21. If your answer to the above is yes, then how long do you expect this parallel process development in 300mm and 450mm will last? Alternatively, if you believe that the advanced nodes will be developed only on 450mm, how do you think you will manage your needs for these advanced nodes?

Q22. What are the areas where 450mm technology development could be leveraged at smaller wafer-scale (modelling & simulation, automation, energy consumption, metrology, etc.)?

Equipment/Material Tools & Technologies, Buildings

Europe is of course a world leader in many equipment technologies, holding many key patents.

Q23. (Equipment and material suppliers) What is the critical mass necessary in your field to bring 450mm technologies to market? Do you have an estimate of the total R&D and pre-production costs associated?

Q24. (Equipment and material suppliers) How long would it take to produce a pilot 450mm tool or compatible product/material from now?

Q25. Under what conditions Europe can participate in such a development? Obviously funding would help anybody but are there any other particular actions that could be performed to speed up development and ensure Europe maintains/attains leadership in your field?

Q26. What kind of partnership needs to be established to fund the development? Please differentiate intra-European cooperation vs. international cooperation requirements if appropriate:

- Between semiconductor manufacturers and equipment/material suppliers?
- Between equipment/material suppliers themselves?

Q27. Although equipment manufacturers operate within their specialist areas, is there an opportunity for co-operation or even mergers to create vertical integration to reduce total costs? Are you working, or do you believe there is scope to work with LCD and PV equipment suppliers who are already mastering very large substrates? Please comment on the degree of cross fertilization that can be done with PV/LCD regarding:

- Large size/volume deposition chambers?
- Large size/volume CVD clusters?
- Large size vacuum pumps?
- Techniques to monitor temperature gradient across large dimension substrates?
- Large size substrate handling?

- □ Manufacturing tool loading/unloading processes?
- □ PV thin film tools?
- □ Specialty gases & bulk gases?
- □ Safety system around gases leaks detection?
- □ Other (Please specify)?

Q28. What are the specifications for equipment/material/process currently available and the one missing to engage 450mm tool development?

Q29. Could you elaborate on any technical challenges related to the development of 450mm in your field, where Europe could leverage its existing strengths in E&M supply (Automation, lithography, metrology, wafer supply, deposition, chemical and gas molecules? Please differentiate between the challenges requiring access to a technological research facility vs. pilot line vs. manufacturing facility.

Q30. (IDMs with 300mm fabs) If you were building a new 300mm fab, do you have the basic design criteria available to build a 450mm compatible fab building? Have you already studied the minimum characteristics of a 450mm fab (shell, DI water, cooling, abatement, power, etc.) needed for 450mm manufacturing? Is there any of this information you can share with us?

Q31. What could be the impact of 450mm manufacturing on energy and resource conservation in your field?

R&D, Semiconductor Technology & Processes

We discussed fab sharing and other schemes earlier but there is another area where increased co-operation could be effective, namely in R&D.

Q32. What are the R&D infrastructures and resources necessary to create 450 mm technologies for a technological research facility (integration line), for a pilot line and for a volume manufacturing facility (Facilities, Fab, manufacturing science, Industrial Logistic, material handling and planning tools)?

Q33. What are the R&D infrastructures and resources necessary to create 450mm technologies for equipment and materials production (Mechanics, optics, chemistry, control, metrology tools for process and facilities monitoring)?

Q34. What would be the benefit and impact of a technological research facility or a 450mm pilot line available in Europe to develop 450mm tools and materials?

Q35. Europe is currently amongst the world leaders in semiconductor research. However it is obvious that the investment being made in CSNE and the move of SEMATECH/ISMI to Albany could threaten this position. How would you ensure Europe's position is maintained through the 450mm transition and beyond? Based on European strategy with regard to 450mm (commitment on manufacturing with 1 or 2 fabs vs. focus on Equipment & Material

technology development), what would be your suggestion regarding the organization of European labs involved in SC Research and Technologies?

Q36. The semiconductor branch is suffering from a lack of attractiveness for young researchers and educated people. What action could be undertaken at national and community levels in order to guarantee that Europe will have enough people with the knowledge and research capabilities being educated?

Q37. What are the key disruptive technological options related to 450mm and below 10nm nodes that could impact the European equipment and material suppliers (EUV, new materials, automation, deposition and metrology)?

Q38. In such a context, what are the capabilities and leaderships Europe can leverage and what are the necessary measures in order to secure European strengths in these domains?

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DECISION
Etudes & Conseil

DECISION
17 rue de l'Amiral Hamelin
75116 PARIS – France
phone: + 33 1 45 05 70 13 fax: + 33 1 45 05 72 65

www.decision.eu

FutureHorizons
The Global Semiconductor Industry Analysts

FUTURE HORIZONS
44 Bethel Road
Sevenoaks, Kent
TN13 3UE – England
phone: +44 (0)1732 740440 fax: +44 (0)1732 740442

www.futurehorizons.com