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Delivering 10X Design Improvements

The endless growth of wireless consumer electronics drives chip design to lower cost and dense mixed-signal functionality, most often on a single chip. Couple this with the requirements of a sensitive RF front-end, and it all becomes a scenario where second order effects become first order--as well as the prime suspects in chip respins and delays to market. In fact, the unintentional and unforeseeable consequences of physical and electrical effects cause the design itself to become a primary source of yield loss.

Another important trend it that the cost, performance, low power and weight requirements of consumer mobile wireless and RF chips is creating a resurgence of custom IC design. We now see chips with a growing amount of analog mixed signal functionality plus complex digital on a single SoC. Designing and verifying these chips is a daunting challenge that is demanding changes in methodology as well as the need to create a class of EDA tools that do not exist today. This next generation of tools must be process and implementation aware with sophisticated analytics to aid designers from design capture through final chip verification.