Nobuaki Miyakawa

Honda Research Institute

3D Stacking Technology and its Application

We have proposed a new 3-dimensional (3D) stacking technology using a wafer-to-wafer stacked method. Electrical conductivity between each wafer is almost 100% and contact resistance is less than 0.7Ω between a through silicon via (TSV) and a bump.

We have also created a prototype of a 3-layer stacking device using our technology, where each wafer for the stacking is fabricated by using 0.18um CMOS technology based on 8-inch wafers.

The device is operated by two times frequency of MCM device case using 2-dimensional devices with identical functions and minimally different power consumption. The yields gotten from the results comprising all functional tests were over 60%.

We have achieved promising results of 3D stacking technology for practical use from our prototype, in particular its applicability for the upturn of the Electronic industry.