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India's LPWAN Network Grows to Meet Smart City Demand

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More Silicon III-V Chips Needed to Enable 5G Devices

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TSMC Boosts Capital Expenditures on 5G

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TALK TO US

European Project Builds 3DIC Exascale Compute Node

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Micron Claims Fastest SSD; Buys AI Startup

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This requires plenty of investment in both networks and the ecosystem, from chips and devices all the way to applications and services. We got a snapshot of this at the LoRaWAN Live conference in New Delhi last week, where we heard about implementations of everything from smart water metering and smart agriculture to smart parking. Under the theme, 'smart tech for a smart sustainable planet', players in the ecosystem highlighted some of their projects and challenges.

Silicon III-V Chips Needed to Enable 5G Devices

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Various organizations, including IBM, the Hong Kong University of Science & Technology, and MIT, have been experimenting with integrating silicon with compound semiconductors to get around such problems.

The electronic devices of the near future will have to contain sensors and transmit data wirelessly to a control center (possibly communicating over a 5G network). This means that they will have to combine RF, low operating power, and a small form factor. A clean and promising approach to achieve all these objectives is to create single chips that combine the capabilities of silicon CMOS with III-V semiconductors.

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TSMC will "probably" increase its 2020 capex from this year's level, according to TSMC CEO C.C. Wei. The company typically waits until the first of each year to forecast its capex for the 12-month period.

Amid the ongoing trade war between the U.S. and China, TSMC appears to be one of the few chipmakers seeing increased demand in China from customers such as Huawei. TSMC said that more than 100 of its over 400 customers are now companies in China.

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The European ExaNoDe project has built what it claims is a groundbreaking compute node prototype paving the way to exascale. It combines a 3DIC with multi-chip-module integration technologies, heterogeneous compute elements with Arm cores and FPGA acceleration, and the UNIMEM memory system, powered by a high-performance, high-productivity software stack.

The ExaNoDe prototype uses 28nm chiplets stacked on a silicon interposer. Detailed modelling and simulation has shown that a realization using state-of-the-art 7nm Arm-core based chiplets with silicon interposer and HBM2 would be a modular, cost-effective and energy efficient avenue to achieve multi-teraflops heterogeneous compute nodes. The project coordinator, Denis Dutoit, a research engineer at CEA-Leti, said, "Affordability and power consumption are the main hurdles for an exascale-class compute node. In the ExaNoDe project, we have built a complete prototype that integrates multiple core technologies: a 3D active interposer with chiplets, Arm cores with FPGA acceleration, a global address space, high-performance and productive programming environment, which will enable European technology to satisfy the requirements of exascale HPC."

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The announcements were made at the Micron Insight conference held at Pier 27 in San Francisco. The conference focused on how to accelerate intelligent systems by improving data access and analysis speed in edge devices.

Micron CEO Sanjay Mehrotra said in his opening remarks at the conference that the company shipped 6 million wafers (including DRAM/3D XPoint/NAND) in fiscal year 2019, which translates into roughly 3 billion solutions for game systems, mobile phones, Internet of things applications, smart factories, and more.