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Synopsys ARC Embedded Vision Processors Deliver 35

Synopsys has launched its latest generation of embedded vision processors with deep neural network (DNN) accelerator delivering what it claims is an industry-leading 35 TOPS (tera operations per second) performance for artificial intelligence (AI) intensive edge applications.

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High-Performance Design for Ultrasound Imaging

In modern medicine, medical imaging has made great strides. Transmitting acoustic energy in the body and receiving and processing the reflections of the signal, ultrasound technology can generate images of our internal organs, map the tissues, and other medical-scientific information.

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Startup Secures IoT with 'Unforgeable' Secure Identities

Crypto Quantique, a London, UK-based startup, uses quantum tunneling to allow devices to have multiple secure 'unforgeable' identities in internet of things (IoT) systems. The company has just raised \$8 million, and also appointed Kumi Thiruchelvam as a co-founder and chief commercial officer.

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TALK TO US



Dell-EMC Include Optane in PowerMax Arrays

TORONTO — Much of the potential of 3D Xpoint technology is expected to come from the DIMM form factor, but Dell-EMC is bullish enough on the Intel Optane SSDs to include it in its latest PowerMax storage array, which also boasts end-to-end NVMe.

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Ceva Goes Automotive with New AI Core & 'Invite'

BRUSSELS, Belgium — A serious number of AI chip startups, many gunning for the automotive market, have popped up in the last few years, but there has been a counterpoint. OEMs and Tier Ones are reportedly eager to design home-grown AI chips — much like Tesla's groundbreaking development of its own "full self-driving (FSD) computer" chips.

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Synopsys ARC Embedded Vision Processors Deliver 35 TOPS

Synopsys has launched its latest generation of embedded vision processors with deep neural network (DNN) accelerator delivering what it claims is an industry-leading 35 TOPS (tera operations per second) performance for artificial intelligence (AI) intensive edge applications. Also introduced is a functional safety processor version for automotive advanced driver assist systems (ADAS), radar/lidar, and automotive sensor system on chip (SoC) development.

Based on the ARCV2 RISC instruction set architecture, the new DesignWare ARC EV7x vision processors feature a 1, 2 or 4-core heterogeneous architecture which integrates vector DSP, vector FPU, and neural network accelerator to enable a variety of intelligent automotive and consumer applications with integrated AES encryption. The optional DNN accelerator scales from 880 to 14,080 MACs to enable a system that delivers up to 35 TOPS performance in 16-nanometer (nm) FinFET process technologies under typical conditions, four times the performance of the previous generation ARC EV6x processors.

High-Performance Design for Ultrasound Imaging

In modern medicine, medical imaging has made great strides. Transmitting acoustic energy in the body and receiving and processing the reflections of the signal, ultrasound technology can generate images of our internal organs, map the tissues, and other medical-scientific information. Ultrasound is represented by a high-frequency sonar system, which measures the tiny echoes of sound waves that pass through the body. The advances in the field of microelectronics have directed the instrumentation towards portable and high-efficiency solutions, with performances that are getting closer and closer to the more complex and decidedly larger systems.

Ultrasound has a wide range of medical applications, including imaging. The main design elements are the transmission and reception of the signal for a correct interpretation of the images. In a pulsed wave (PW) ultrasound system, a high voltage pulse stimulates the piezoelectric transducer (a crystal), causing a corresponding mechanical compression (an inverse piezoelectric effect), and thus creating the ultrasound wave that passes through the body.

Startup Secures IoT With 'Unforgeable' Secure Identities

Crypto Quantique, a London, UK-based startup, uses quantum tunneling to allow devices to have multiple secure 'unforgeable' identities in internet of things (IoT) systems. The company has just raised \$8 million, and also appointed Kumi Thiruchelvam as a co-founder and chief commercial officer.

Having debuted its technology in Barcelona last fall, the company said it uses the most advanced techniques in cryptography and quantum physics to address the growing challenges of end-to-end IoT security. Using its quantum driven secure chip (QDSC), Crypto Quantique (CQ) said it enables devices to regenerate keys without secure storage, and also to identify themselves to remote servers without a previous trust relationship or shared key being needed.

Dell-EMC Include Optane In PowerMax Arrays

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The company's updates to PowerMax introduce storage class memory (SCM) as persistent storage via dual-port Intel Optane SSDs. In a telephone interview with EE Times, Caitlin Gordon, vice president of product marketing at Dell-EMC, said the dual-ported drive provides built-in resiliency for the storage platform, and reflects a close collaboration with Intel.

The key value proposition for PowerMax with dual-port Intel Optane SSDs is latency, she said. "This is all about achieving the right response times out of the drive." Those response times have been achieved in the lab for some time, and as a lead development partner, Dell-EMC's focus has been on getting the resiliency of the firmware to where it needs to be, said Gordon.

Ceva Goes Automotive With New AI Core & 'Invite' API

BRUSSELS, Belgium — A serious number of AI chip startups, many gunning for the automotive market, have popped up in the last few years, but there has been a counterpoint. OEMs and Tier Ones are reportedly eager to design home-grown AI chips — much like Tesla's groundbreaking development of its own "full self-driving (FSD) computer" chips.

If the latter case is the trend, where does it leave IP core licensors like Ceva, Inc.? And what should they do next?

First and foremost, they must increase the performance of their licensable IP cores designed for AI architecture. They need, above all, to make their neural network cores even more irresistible to SoC designers.