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TALK TO US

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Limitations of 3D NAND Scaling

The life span of 3D NAND might be a lot shorter than most people think.
At the Flash Memory Summit this year, Samsung announced its development of 1Tb 3D NAND, which would be used for commercial products launching next year. However, I wonder when the 4Tb 3D NAND will hit the market.

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WD Gives Hard Drives New Spin

SAN JOSE, Calif. — Western Digital demonstrated a new technology for recording heads it claims will keep hard disk drives spinning for years to come. It will ship by mid-2019 drives using microwave-assisted magnetic recording (MAMR), a technology it expects can lead to 40 TByte drives by 2025.

The technique was born in a Carnegie Mellon lab in 2006. WD struggled for years to implement the technique until two years ago when a researcher at the former IBM plant here where the hard drive was born had an "a-ha moment" that paved the way to commercial products.

Foundries Target China

SAN FRANCISCO — China is expected to account for 13 percent of sales for the world's pure-play chip foundries in 2017, up from 12 percent last year, as the country's fabless semiconductor activity continues to accelerate.

Pure play foundry sales in China are expected to reach $7 billion in 2017, up 16 percent from 2016. The growth rate is more than double the overall growth rate for global pure play foundry sales, the research firm noted.

TSMC is forecast to hold about 46 percent of the market for China's pure play foundry sales with sales of about $3.2 billion, up 10 percent from 2016.

Future Auto Radar Goes Back to Analog

MADISON, Wis. — Many carmakers, in order to increase the real-world situational awareness of their highly automated vehicles, have already accepted the necessity of literally surrounding every chassis with different types of sensors. What's not given, however, is the quality of these sensors. How good, for example, are vision, lidar and radar sensors today, and how much better do they have to get?

Metawave Corp., spun out of PARC, a Xerox company based in Palo Alto, Calif., thinks it can alter what the automotive industry perceives as the "limitations" of conventional radars. Today, automotive radars can't see faraway objects and can't discriminate what they see. They operate at processing speeds that aren't fast enough for the highway.

In short, today's automotive radar can't see objects that a camera or lidar can see. Its only saving grace is that it operates in all-weather conditions.

Apple Watch Packs Qualcomm LTE

SAN JOSE, Calif. — Qualcomm supplied the LTE modem in the Apple Watch Series 3 as well as a handful of other wireless chips, according to a teardown from TechInsights. The latest watch appears to continue to push the boundaries of system-in-package design, packing a dozen major chips and dozens of discretes.

The new watch uses the same size SiP as the existing device. However, the Series 3 clearly packs more components, TechInsights said.

TechInsights found the Qualcomm MDM9635M, a Snapdragon X7 LTE modem in the 42mm sport band model A1861 with GPS + cellular it opened up. The same LTE chip appeared in the iPhone 6S/6S Plus, the Samsung Galaxy S6 Edge and other handsets. The modem was mated in a package-on-package with a Samsung K4P1G324EH DRAM in the watch.

Limitations of 3D NAND Scaling

The life span of 3D NAND might be a lot shorter than most people think.

At the Flash Memory Summit this year, Samsung announced its development of 1Tb 3D NAND, which would be used for commercial products launching next year. However, I wonder when the 4Tb 3D NAND will hit the market.

Based on the information available on TLC 512Gb 3D NAND with 64-layer on about 130mm2 die size (from Samsung and Toshiba) and assuming string stacking of 64-layer, I figured that in order to implement the 4Tb NAND chip:

Eight string stacks of 64-layer are needed. Which will make (512Gb x 8) = 4Gb

The total layer then becomes 512-layer on 130mm2 die size

It will take about a year to process a wafer, 5 weeks for memory logic plus 8 times (i.e. 8 string stack of 64-layer) 5 to 6 weeks for a 64-layer cell layer implementation. Therefore, the wafer processing time for a 512-layer will be about 45 to 53 weeks.