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Cerf Calls for Improved IoT Software

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TALK TO US

Arm Ready to Sacrifice Profits for Long-Term IoT Growth

Arm is better positioned as a privately held company to take a strategic approach for long-term growth as it addresses the IoT market, according to Rajeev Misra, CEO of SoftBank's $100B Vision Fund and a director of the SoftBank Group.

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AI Startup Seeks its Voice

SAN JOSE, Calif. — Battery-powered devices will get a new option for hardware-accelerated speech interfaces next year if Kurt Busch makes his targets this year.

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Cerf Calls For Improved IoT Software

SAN JOSE, Calif. — The Internet of Things won't live up to its promise unless engineers redouble their efforts to develop high quality, secure and interoperable software. Even then, new programming techniques and even legislation may be needed.

That's the message Vint Cerf, a co-developer of the Internet Protocol and chief Internet evangelist for Google, shared with colleagues at a recent technical gathering.

"We should be extremely thoughtful about the quality of IoT software. People are relying on these things to work autonomously, and these days almost anything can become a programmable, communicating device because the chips are so inexpensive," Cerf told EE Times in an interview.

Imec Demonstrates MRAM Manufacturability

LEUVEN (Belgium), June 18, 2018 – At this week's 2018 Symposia on VLSI Technology and Circuits, imec, the world-leading research and innovation hub in nanoelectronics and digital technology, demonstrates for the first time the possibility to fabricate state-of-the-art spin-orbit torque MRAM (SOT-MRAM) devices on 300mm wafers using CMOS compatible processes. With an unlimited endurance (>5x1010), fast switching speed (210ps), and power consumption as low as 300pJ, the SOT-MRAM devices manufactured in a 300mm line achieve the same or better performance as lab devices. This next-generation MRAM technology targets replacement of L1/L2 SRAM cache memories in high-performance computing applications.

SOT-MRAM has recently emerged as a non-volatile memory technology that promises a high endurance and low-power, sub-ns switching speed. With these properties, it can potentially overcome the limitations of spin-transfer torque MRAM (STT-MRAM) for L1/L2 SRAM cache memory replacement. But so far, SOT-MRAM devices have only been demonstrated in the lab. Imec has now for the first time proven full-scale integration of SOT-MRAM device modules on 300mm wafers using CMOS-compatible processes.

NXP Announces Automotive Processors in S32 Family

SANTA CLARA, Calif. — Eight months after announcing its "whole vehicle" automotive processing platform last October, NXP used its annual NXP Connects conference here last week to announce a new family of processors to manage the systems that accelerate, brake and steer vehicles safely, whether under the direct control of a driver or an autonomous vehicle's control.

The new 16nm 800MHz NXP S32S microcontrollers meet the needs of carmakers developing future autonomous and hybrid electric vehicles, and the company claims to offer the highest performance ASIL D capability available today.

The key focus is on safely and securely acting in autonomous environments, which is why the company decided to use the new Arm Cortex-R52 cores, according to Ray Cornyn, responsible for vehicle dynamics and safety products at NXP.

Arm Ready To Sacrifice Profits for Long-Term IoT Growth

LONDON — Arm is better positioned as a privately held company to take a strategic approach for long-term growth as it addresses the IoT market, according to Rajeev Misra, CEO of SoftBank's $100B Vision Fund and a director of the SoftBank Group.

"IoT requires an entire stack, not just the chip, and in order to make these investments, you need to sacrifice profits over the next three to five years," Misra said here this week at CogX, one of the biggest artificial intelligence conferences in the U.K. "It takes courage to take a long-term view when shareholders look for nearly 10% growth per year."

AI Startup Seeks Its Voice

SAN JOSE, Calif. — Battery-powered devices will get a new option for hardware-accelerated speech interfaces next year if Kurt Busch makes his targets this year. The chief executive of Syntiant aims in 2018 to sample a novel machine-learning chip and raise a Series B to make it in volume.

The startup is designing a 20 tera-operations/watt chip using 4- to 8-bit precision to speed up AI operations initially for voice recognition. It uses an array of hundreds of thousands of NOR cells, computing TensorFlow neural-network jobs in the analog domain.

Syntiant will release a reference design pairing its sub-watt chip with an Infineon MEMS microphone. If it is successful, the two will collaborate on other designs. "We want to make it extremely easy to add voice control to any kind of device," said Busch.