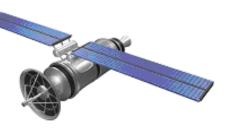
# FutureHorizons



## The Global Semiconductor Industry Analysts

### **FH MONDAY**

12 March 2018

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## **Future**Horizons









#### B'com's Jericho2 Rides 2.5D Stack

Broadcom's latest communications processor rides a 2.5D chip stack with HBM2 memory. Jericho2 uses the boost in memory bandwidth to leapfrog the performance of OEM ASICs in high-end switches and routers.

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## Arm GPU Gets More Al Muscle

SAN JOSE, Calif. — ARM announced four new cores for mainstream smartphones and digital TVs, two Mali GPUs and associated video and display cores for them.

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#### Teardown: ST Grows Inside Samsung's S9

PARIS — Some gadget pundits are already writing off Samsung's new Galaxy S9, scheduled for roll out next week, as being "too predictable" or "just too similar" to last year's Galaxy S8.

As far as its look and feel are concerned, indeed, there is little argument.

But Romain Fraux, chief technology officer at System Plus Consulting (Nante, France), told us that his team, who just finished the preliminary teardown of the S9 handset (designed for the European market), has observed several hardware innovations in S9. System Plus is Lyon, France-based Yole Développement's reverse-cost engineering partner.

#### **Chirp Slurped Up By TDK**

BARCELONA — Chirp Microsystems, a Berkeley, California-based startup with 15 employees, which launched only a year ago at the Mobile World Congress its first high-accuracy, ultra-low-power ultrasonic sensing development platform, returned to Barcelona this week with a deal in hand to be acquired by Japan's TDK Corp.

TDK's Board of Directors approved the transaction on Feb. 28, and the closing is expected in the following days.

Chirp is hopeful that the deal with TDK will create an opportunity for the startup team to accelerate the growth of its ultrasound technology across several markets ranging from automotive and IoT to home and mobile devices.

#### **IoT Security Concerns Push Vendors To The Edge**

NUREMBERG, Germany — Doing more processing at the edge to avoid sending sensitive data to the cloud emerged as a common theme among vendors at the Embedded World conference here last week. Whether this is a result of forthcoming GDPR (General Data Protection Regulation) laws coming into force across the European Union on May 25, or whether there it is simply a lack of sufficient security in current devices is difficult to tell.

A recent report on IoT cybersecurity readiness certainly points to the latter. Lawrence Munro, vice president SpiderLabs at Trustwave, who released the IoT Cybersecurity Readiness Report, said, "As IoT adoption continues to proliferate, manufactures of IoT are sidestepping security fundamentals as they rush to bring products to market. We are seeing lack of familiarity with secure coding concepts resulting in vulnerabilities, some of them a decade old, incorporated into final designs.

#### B'com's Jericho2 Rides 2.5D Stack

SAN JOSE, Calif. — Broadcom's latest communications processor rides a 2.5D chip stack with HBM2 memory. Jericho2 uses the boost in memory bandwidth to leapfrog the performance of OEM ASICs in high-end switches and routers.

The chip expands into networking the packaging technology pioneered by AMD, Nvidia, and Xilinx in high-end FPGAs and graphics processors. With its StrataDNX Jericho2, Broadcom also takes a small step toward open-programming environments by providing C++ tools for the chip to select customers.

#### **Arm GPU Gets More Al Muscle**

SAN JOSE, Calif. — ARM announced four new cores for mainstream smartphones and digital TVs, two Mali GPUs and associated video and display cores for them. The news shows that Arm is, at least for now, taking a three-tier approach to machine learning and that China mobile OEMs are becoming increasingly influential.

Arm's new Mali G52 GPU core is aimed at mid-tier smartphones and digital TVs using combinations of Cortex-A72 and -A55 CPU cores. The GPU boosts machine-learning performance up to 3.6x for ImageNet classifiers compared to its existing G51 core.

The G52 packs eight execution engines compared to four on the G51, with four lanes in each engine and each capable of up to four 8-bit integer multiply-accumulate operations per cycle. Up to four G52s can be used in an SoC, each executing up to 288 MACs/cycle.