Coordination Action to enable an effective

European 450 mm Equipment & Materials Network

Enable 450 Newsletter

Issue 10 **May 2015**

Enable450 Newsletter

Welcome to the tenth newsletter for the Enable450 project. You may have noticed it is some time since issue nine but there simply isn't the amount of activity in 450mm technology occurring to make it be needed more regularly.

If you would like to supply information for publication, please contact the editor at mbryant@futurehorizons.com.

Our website is available to allow previous issues to be downloaded.

http://www.enable450.eu/index.html

Please distribute this document to anyone who might be interested and you may place it on your own intranet if you wish.

Overview

450mm wafer technology remains out of the main focus of the industry for now, with as soon as the 20nm technology started shipping, interest moved straight onto the 14nm node.

However to produce these nodes still requires more advanced processing technology and so we are definitely seeing the research at G450C and on European 450mm related research projects beginning to be used on advancing 300mm processing equipment and materials.

In previous issues we have highlighted the contribution Europe has made to the Notchless Wafer standard, primarily through the efforts of RECIF Technologies, and to the smaller edge exclusion zone. Both techniques increase the number of die that can be fabricated on a wafer. An interesting rumour currently circulating is that one major semiconductor manufacturer has been asking its suppliers what would be the implications of applying these two techniques to 300mm wafers so as to weigh up the benefits against cost.

Obviously this may be nothing more than simple 'bar talk', but it would be an interesting spin-off development from the 450mm programmes.

SEMICON Europa 2015

The SEMICON Europa 2015 will take place in Dresden from October 6th to 8th 2015. There will not be a dedicated session on 450mm technology this year but the Semiconductor Technology Conference (STC) "Productivity Enhancements for future Technology Nodes" will include updates on 450mm technologies.

If you wish to submit a paper for this, applications close shortly so you will need to rush.

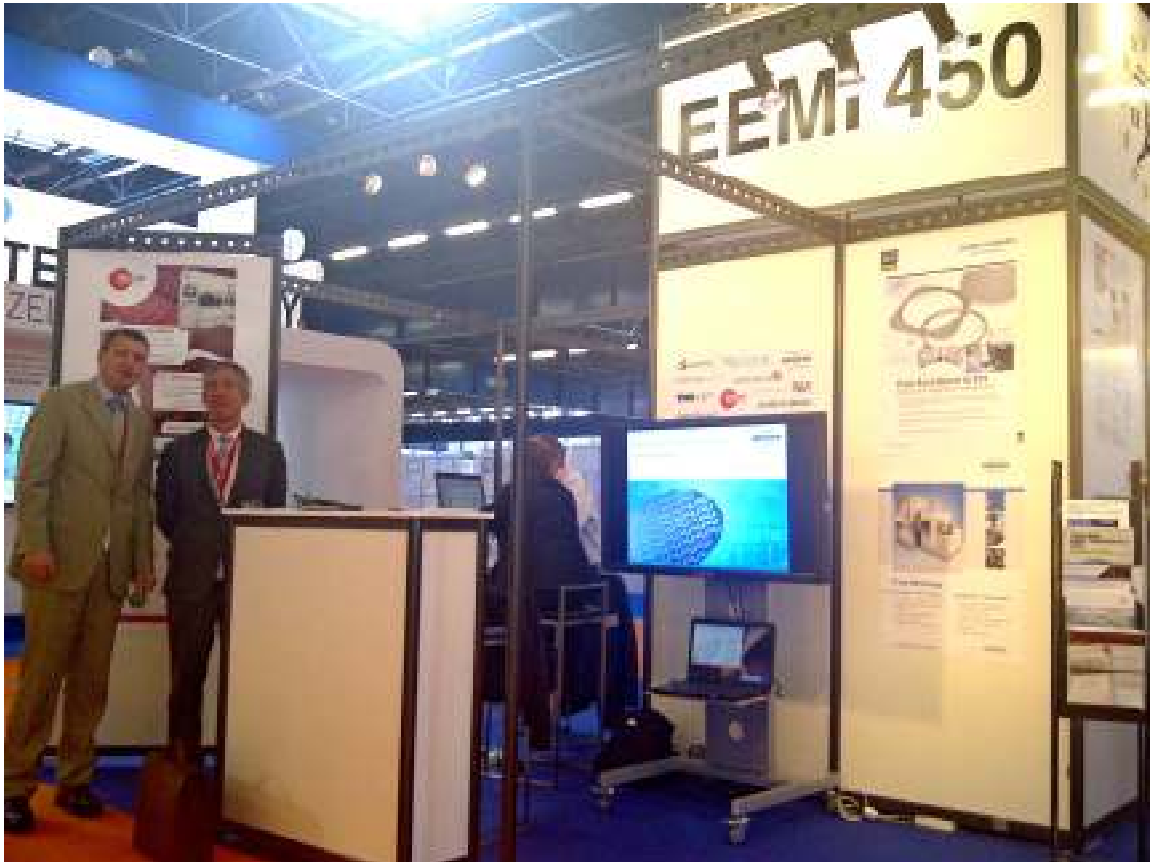
http://www.semiconeuropa.org/

EEMI450 & G450C Collaboration

As usual, meetings were held between EEMI450 and G450C. Progress on the previously agreed Cross Collaborative approach was discussed and is already being deployed by RECIF with the tool they installed at Imec. All results gained there will be recognized by G450C so as to avoid duplication of effort.

EEMI450 Booth

In 2014 SEMI Europe organized a booth on behalf of EEMI450 at SEMICON Europa which was funded by the Enable450 project. This was well received but the project doesn't have the funds available this year but if you are interested in participating in a paid-for stand contact Bas van Nooten or the editor of this newsletter.



EEMI450 GA 2015

It was intended to have the annual General Assembly of the EEMI450 in April but unfortunately this had to be cancelled.

However RECIF have kindly provided their intended slide-set for publication here.

NGC450

update for
General Assembly EEMI450
April 2015

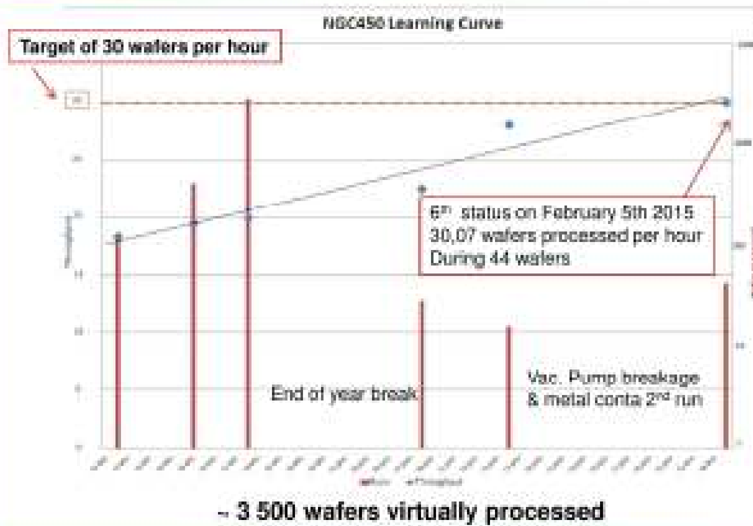
Hardware integration

Handling platform installed at imec in September 2014

Software integration

3

Learning curve improvement



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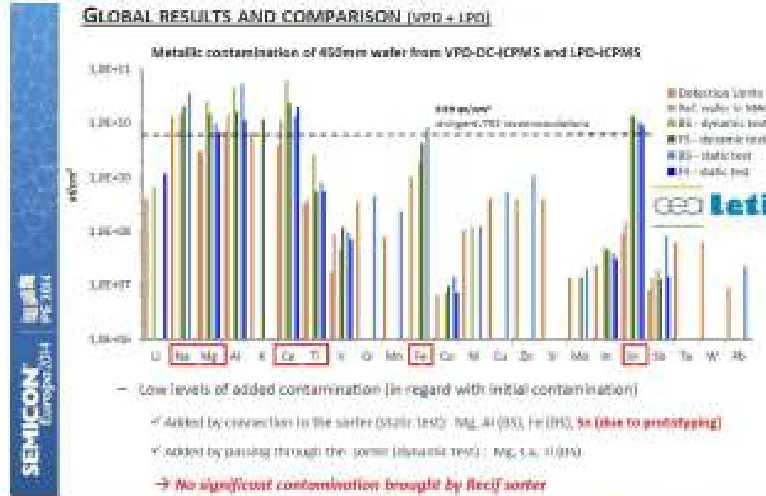
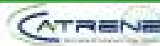
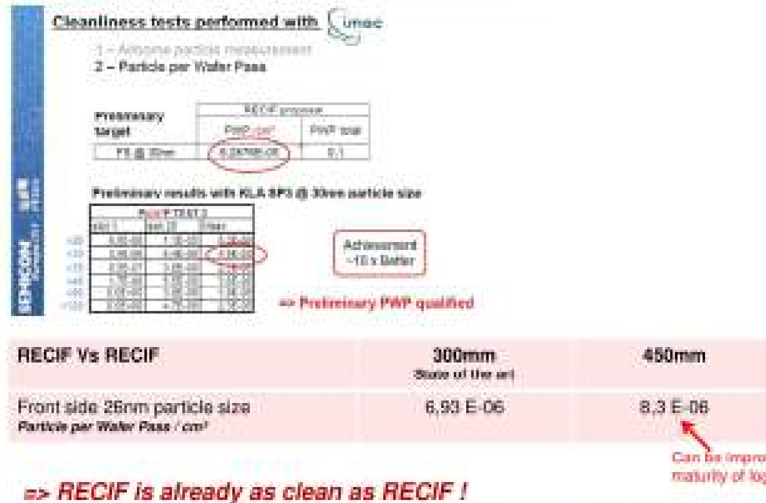

Metal Ion Contamination charac' (CEA Léti)
GLOBAL RESULTS AND COMPARISON (VPD + LPD)
Metallic contamination of 450mm wafer from VPD-DC-ICPMS and LPD-ICPMS
Low levels of added contamination (in regard with initial contamination)
→ No significant contamination brought by Recif sorter




Particle contamination charac' (imec)
Cleanliness tests performed with imec
2 – Particle per Wafer Pass
Preliminary results with KLA SP3 @ 30nm particle size
=> Preliminary PWP qualified
RECIF Vs RECIF
300mm
450mm
Front side 26nm particle size
Particle per Wafer Pass / cm²
6,93 E-06
8,3 E-06
Can be improved with maturity of logistics
=> RECIF is already as clean as RECIF !

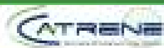
Continuation

These results will now support further collaborative work within and outside Europe

Next steps are:
- Notchless wafer alignment module

- Demonstration Test Methodology with G450C @ imec

- Advanced characterization for 10nm



NGC450 project ended on a complete technical success.

RECIF thanks all its partners !

450 Millimeters of News

G450C Lithography Installation

On April 16, 2015 it was announced that installation of the world's first ever 450mm Immersion Scanner has begun at the SUNY Polytechnic Institute's Albany NanoTech Complex.

Nikon Corporation made the machine in Japan where it was first tested to produce fully exposed 450mm wafers, and then shipped to Albany for installation there by a team of more than 50 engineers from the U.S. and around the world.

Toshikazu Umatate, Nikon Corporation Senior Vice President and General Manager of the Semiconductor Lithography Business Unit said, "The Nikon 450mm program is progressing steadily and this exciting milestone was made possible by close collaboration with our many partners throughout the consortium. Nikon is committed to continuous lithography innovation and advancement, and supporting the industry in achieving the next generation of semiconductor manufacturing."

450mm Central

The SEMI 450mm website has two new papers available. These are "300mm & 450mm Standard Calibration Wafers", presented by Rand Cottle of G450C, and "Metallic Contamination Analysis of 450mm Wafers using VPD-DC-ICPMS & LPD-ICPMS", presented by C.Agraffeil of CEA-LETI.

http://www.semi.org/Issues/450mm

450mm.com

There is one new article on this site concerning a potentially better way of making larger wafers.

http://450mm.com/blog/2015/04/12/cz-hard-truths/

450mm Standards Update

In February, SEMI again updated their standards page at

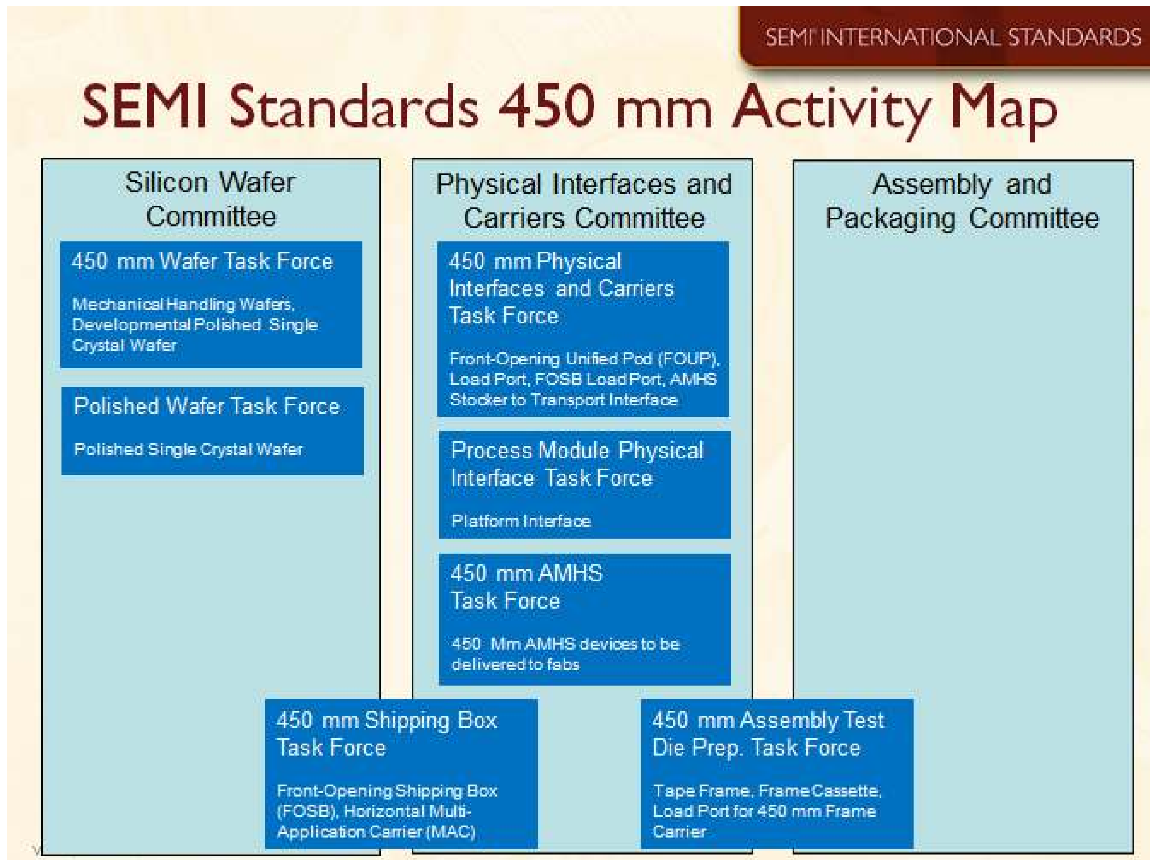
http://www.semi.org/en/node/41211

The new addition is

450 mm Polished Single Crystal Silicon Wafer Specification

SEMI M1-0215 – Specifications for Polished Single Crystal Silicon Wafers was revised and published in October 2014. The new edition includes a significant addition of a 450 mm polished single crystal polished wafer specification and the guide for specifying 450 mm wafer for 32, 22, and 16 nm technology generation. Today, the specification requirements for 450 mm diameter wafers are much more extensive that those of previous smaller diameters. Standardized parameters include edge profile, warp, conductivity, dopant, and surface conditions.

This image shows where 450 mm standards development is taking place :



10/100/20

The 10/100/20 initiative was announced by Commissionaire Neelie Kroes in 2013 and aims to achieve 20% of world semiconductor production within Europe by 2020.

Since then the new European Commission President, Jean-Claude Juncker of Luxembourg, has instigated the new European Fund for Strategic Investments (EFSI) under which Important Projects of Common European Interest (IPCEI) will operate in many key industries, amongst which is semiconductors.

The fund size is €21 billion but it is hoped this will release up to €315 billion in other investments. The money was redirected from the Horizon2020 research funding budget, raising the ire of University leaders across Europe, many of whom had become rather over-dependent on European funding rather then from their own country governments.

In the semiconductor field a number of IPCEI projects are being considered, including one that will be examining the economics of the 450mm wafer size in great detail to determine whether to include it in their plans or not. It is expected that the first submissions will be made early in 2016 for approval later that year.

Editorial

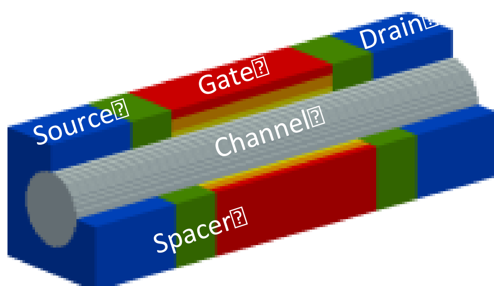
Any views expressed here are those of the editor and not necessarily of other European 450mm project members.

As we've mentioned in previous newsletters, if it is to occur the transition to a 450mm wafer size cannot ignore the process node it is being introduced at. But as the introduction of each new node becomes ever harder, the additional problem of introducing a larger wafer size becomes ever more expensive and daunting. Here Professor Asenov of Glasgow University and Gold Standard Simulations discusses some issues which have to be addressed in transistor design for upcoming nodes over the next decade.

Nanowire Transistors Can Offer Clean Run Down 5nm CMOS

While Intel is ramping up its second generation (14nm) FinFET technology and 16/14nm FinFET CMOS is about to enter volume production at the major foundries, the next generation transistors suitable for 7nm CMOS and below are already on the drawing board. One of the best candidates "Gate all around" transistors, better known as nanowire transistors (NWT), have superior scaling properties compared to FinFETs and can be scaled to channel lengths of approximately 5nm. The expected introduction of new channel materials like SiGe, Ge and III-Vs are also critical to ensure that transistor performance continues to be enhanced.

In NWTs the gate is wrapped all the way around the conducting channels as illustrated in Fig. 1. Because of this it can control better the current flow compared to bulk, FDSOI and FinFET transistors offering steeper subtreshold slope and hence less leakage current. Drive current can be enhanced due to confinement induced band splitting. Multiple nanowires can be packaged in the same transistor to increase the drive current at the same pitch as illustrated in Fig. 2. This is equivalent to an increase of the fin height.



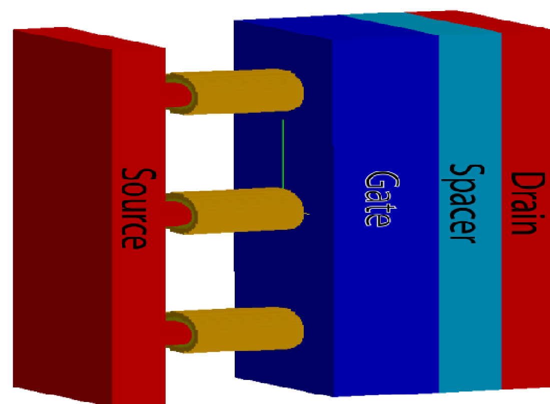


Fig. 1 Schematic view of single channel all gate around Nanowire Transistor NWT.

Fig. 2 Multiple channel NWT.

However, this will not be a smooth ride. The operation of CMOS transistors at 7nm and beyond is extremely complex due to strong quantum mechanical effects and quasi-ballistic transport.

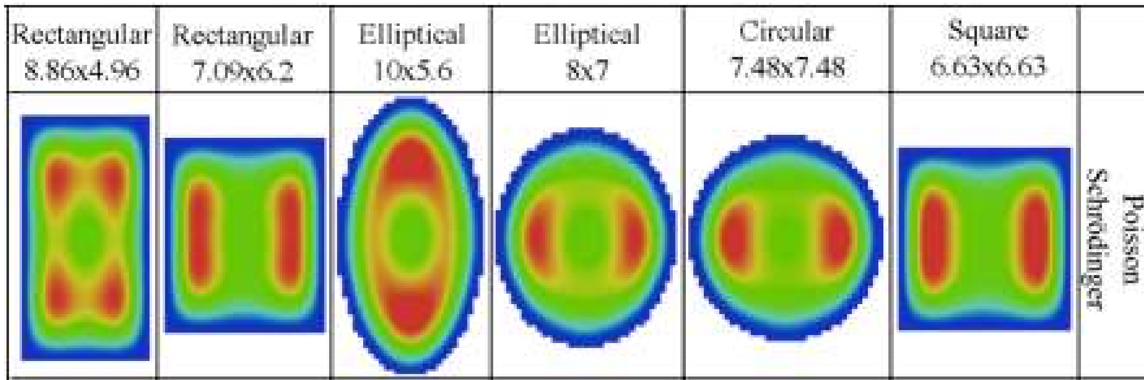
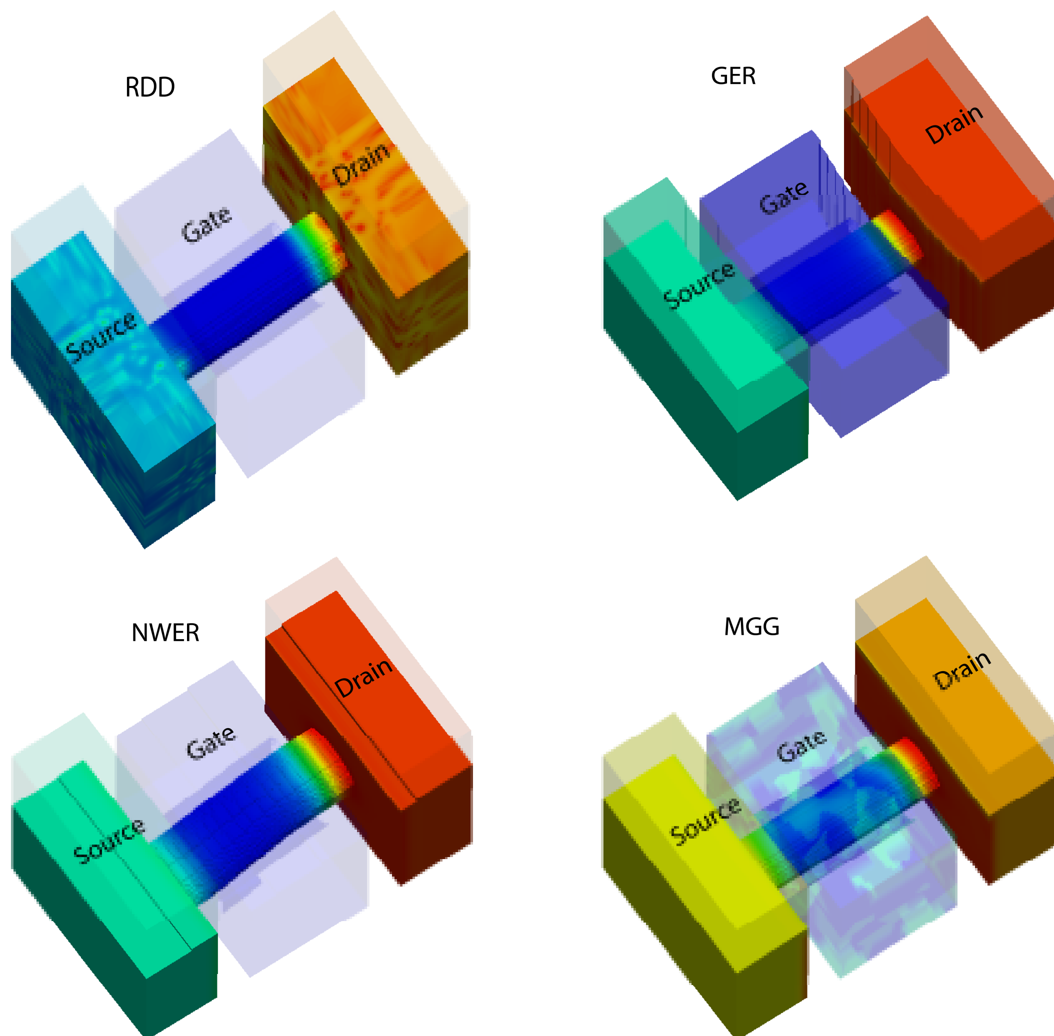


Fig. 3 Mobile charge distribution in a NWT with different cross sections suitable for 7nm CMOS technology. Due to quantum mechanical confinement effects 'strange' patterns determine the positions of the current flow in the nanowire cross section.

You do not need to be an expert in quantum mechanics in order to understand the intricacy of the optimal nanowire transitory design due to quantum confinement effects. Fig. 3 illustrates the mobile charge distribution in a NWT with differen cross sections suitable for 7nm CMOS technology. In red are the regions with high carrier concentration where the current will flow. The pattern of these regions is determined by the quantum confinement effects and is different for different nanowire and substrate orientations. Although all different nanowires in Fig. 3 have the same cross section the elliptical 10x5.6 nm nanowire have 20% more charge, compared to the square 6.63x6.63nm NWT. Far from obvious, but a wrong choice of the NWT cross section can kill performance compared to the competition.

Let us offer some more entertainment and parity pictures. The NWT transistors will not escape the 'curse of the very small'. They will be as susceptible as ever to local, statistical variability. Fig. 4 illustrates how NWT will be affected by random discrete dopants (RDD), gate edge roughness (GER), fin edge roughness (FER) and metal gate granularity (MGG).



So, after all, the development of the next generation NWT technology will be very challenging as large combinations of transistor design parameters, channel materials and gate dielectrics need to be evaluated, a very expensive process. Sub-optimal technology decisions could literarily bankrupt even the largest technology foundry in this $10B+ new world of CMOS technology development. Additionally, the complexity and uncertainty of future technology also profoundly affects fabless and IP development companies, which have to prepare their designs for the new technology solutions years in advance.

Advanced, predictive TCAD is the answer to many of the above challenges. For example the state-of-the-art GSS 'atomistic' simulator GARAND can predict the characteristics of NWT, including quantum mechanical & non-equilibrium transport effects as well as global and local variability. The best in class quantum simulation and correction technologies accurately capture the impact of quantum effects on the performance of

NWTs. The ensemble Monte Carlo (EMC) transport module of GARAND, which includes multi sub-band EMC, predicts accurately the performance of these future devices based on the electronic properties of different channel materials.

Such tools allow fast screening of future technology options and ensures that the right technology decisions are made as early as possible in the development cycle.

Once decisions are made, the tool chain needs to allow fast development of accurate early PDKs. This facilitates fabless companies in making the best technology choices according to their specific product requirements. Once the technology is chosen it can then be optimised for particular applications using an automated tool chain, giving an invaluable differentiator within a highly competitive market.

Conclusions

The editor has known Professor Asenov and his team at Gold Standard Simulations for many years. Thanks to support on many projects from the European Union funded FP7 and ENIAC programmes they have become a world leading supplier of predictive simulation nano-CMOS devices including statistical variability and reliability. Their simulation tool chain enables the physical simulation of performance and statistical variability and reliability in contemporary and future CMOS technologies, statistical compact model extraction and statistical circuit simulation using “push button” cluster-based technology.

The cases of GSS and RECIF Technologies featured earlier in this issue highlights just how much SMEs can gain from these EU funded programmes and those not engaging in them really should reconsider.

Regarding Professor Asenov and GSS, I can attest to their willingness to engage in intellectual debate on all matters of advanced semiconductor design far beyond their core skill of variability. If you are attending the DAC conference in San Fransisco from June 7 to 11, I would strongly recommend you drop in on the GSS stand 3114 and hear their latest thoughts in person.