



**Coordination Action to enable an effective
European 450 mm Equipment & Materials Network**

Enable 450 Newsletter

Issue 8

Summer 2014

Enable450 Newsletter

Welcome to the eighth newsletter for the Enable450 project.

If you would like to supply information for publication, please contact the editor at mbryant@futurehorizons.com.

Our website is now up to allow previous issues to be downloaded.

<http://www.enable450.eu/index.html>

Please distribute this document to anyone who might be interested and you may place it on your own intranet if you wish.

Overview

With the introduction of new processes from all the major players the industry hasn't been talking about 450mm so much in recent months, but this does not mean the topic has 'gone away' and progress is still being made. However the efforts involved in introducing the new processes has diverted attention away from larger wafers and so some delays can be expected. To match this, the Enable450 and Bridge450 projects have been extended by a year with an end-date of November 2016. But as the available budget remains the same the time between these newsletters will be stretched a little. We hope this doesn't detract from making this newsletter a useful resource for our readers.

SEMICON Europa 2014

SEMICON®
Europa2014

October 7–9
Grenoble, France

The SEMICON Europa 2014 event will take place in Grenoble from October 7th to 9th, following on from SEMICON Taiwan which will be taking place just as you receive this newsletter. We hope to include details of both conferences in the next newsletter.



For the first time the EEMI450 initiative will have their own stand number 1543 in “Allée des Clusters”, where you can come and meet representatives of some of the companies involved and discuss their progress to date on the various funded R&D projects. If you discover that your own company isn’t a member of EEMI450 and should be then we can also arrange for the appropriate paperwork to be sent to the relevant person.

450 mm Innovations and Synergies for Smaller Diameters

There will also be presentations in four sessions spread over 2 days on 450mm wafers entitled “450mm Innovations and Synergies for Smaller Diameters”. An outline of the presentations are detailed below.

Session 1 Worldwide Consortia and Research Institute updates – Wed Oct 8th

13:30 Opening Remarks - Lothar Pfitzner, Fraunhofer IISB

13:35 Continued Progress on 450mm Development - Frank Robertson, VP/GM, G450C

14:05 Title to be confirmed - Lode Lauwers, Imec

14:35 Sustainability challenges in the 450mm technology node - Adrian Maynes, F450C Program Manager, Facilities 450mm Consortium (F450C)

14:55 Scaling Options in Relation to 450mm - Michael Liehr, Executive VP for Innovation & Technology, CNSE

15:15 450mm synergies for smaller wafer diameters: contamination control - Olaf Kievit, Projectmanager, TNO

Session 2 European Commission, Public Authority funding opportunities and project example

16:30 Research and Innovation on 450 mm and related topics: A European Perspective - Willy van Puymbroeck, Head of Unit A4 Components, European Commission

17:00 450mm specifications will boost the 300mm yield in wafer manufacturing - Denis Rousset, Office Director, CATRENE

17:20 Semiconductor Equipment Assessment for Key Enabling Technologies (SEA4KET) - Markus Pfeffer, Group Manager, Fraunhofer IISB

Session 3 Status of 450mm Equipment and Materials – Thur Oct 9th

09:05 The dawn of 450mm production: Batch and single wafer equipment and process exploration - Cornelis Herbschleb, Process Engineer, ASM Europe BV

09:35 AMC contamination management strategy for 450mm - Magali Davenet, R&D Collaboration and Funding Manager, adixen Vacuum Products

09:55 Upsizing Wafer Fab UPW Needs to 450mm Demands - Hanspeter Mueller, Microelectronics Manager, Georg Fischer Piping Systems

10:15 Innovative Semiconductor Solutions supplied out of Silicon Saxony - Jochen Kinauer, Director Business Development/ Sales Semiconductor, AIS Automation Dresden GmbH

Session 4 Status of 450mm Equipment and Materials, and opportunities for other technologies

11:30 450mm progress - toward cross collaboration & cross utilization - Guilhem Delpu, Product marketing & collaborative programs, RECIF Technologies

12:00 450mm - it's more than abatement, it's the solution. - Mike Czerniak, Product Marketing Manager, Edwards

12:20 Early production testing of 450mm process modules - Mike Cooke, CTO, Oxford Instruments

12:40 FOUP (Pod) contamination control solutions for 200mm, 300mm and 450mm substrates. - Jorgen Lundgren, Senior Field Applications Engineer, Entegris GmbH

Each session includes time for questions to the speakers at the end of the session.

Full details are at :

http://www.semiconuropa.org/ProgramsandEvents/Semiconductor/CTR_030444

Registration to attend can also be made on the SEMI Europe website

450 Millimeters of News

Progress on TSMC's planned 450mm fab

A special panel of the Environmental Protection Administration (EPA) has approved the environmental impact assessment for a piece of land designated for construction of a 450mm fab by TSMC in Taichung, central Taiwan. The fab is part of the planned expansion project of the Central Taiwan Science Park (CTSP). The expansion project will occupy a land area of up to 53 hectares and will accommodate TSMC, Giant and other companies. The project is still subject to approval by the plenary session of the EPA as well as the Construction and Planning Agency under the Ministry of the Interior (MOI), according to CTSP.

TSMC is expected to be able to start constructing the 450mm fab at the start of 2015 at the earliest, the Chinese-language Economic Daily News (EDN) quoted sources at CTSP as saying.

TSMC's total investments for the fab are expected to reach US\$16 billion, said the paper. Other sources have also indicated that the expansion project will create 7,000 job opportunities and a production value of NT\$200 billion a year when completed in 2019.

However, TSMC said it has not yet set a timetable for construction of fab.

Bridge450 US and Asian Presentations

The Bridge450 team has gathered information on most European companies involved in 450mm technology and the first presentations have been made to American companies on European abilities in both 450mm and advanced 300mm wafer processing. Similar presentations will be made to key Asian companies later this year whilst trying to find any information on the TSMC fab, and then feedback will be made to the European companies.

About BRIDGE450

Bridge450 is a work program defined under the Objective FP7-ICT-2013-11 "An action to develop a European strategy which addresses the challenges in manufacturing for 450 mm in dialogue with G450C and with the US, Korea and Taiwan." It is effectively a sister project to Enable450 and shares many of the same resources, but its members are mostly SMEs on whom the project focuses.

Notchless Wafers

The adjudication on standards for Notchless Wafers intended to be made at SEMICON West has now been postponed until the next meeting during SEMICON Europe to allow TSMC to provide a final wording the IP clearance. RECIF have been representing the views of European equipment manufacturers on this topic so please contact them for more details if needed.

World's First Fully Patterned 450mm Wafers Unveiled at SEMICON West

The world's first fully patterned 450mm wafers were revealed at SEMICON West and were on display throughout the 3-day event in San Francisco, California.

http://www.g450c.org/CNSE_Nikon_Semi_Wafer_PR.docx

Nikon 193i 450mm Scanner

At the recent SEMICON West, Nikon confirmed that a system is on schedule to be delivered to the G450C at Albany in early 2015.

G450C LITHOGRAPHY EQUIPMENT PROGRESS **G450C**

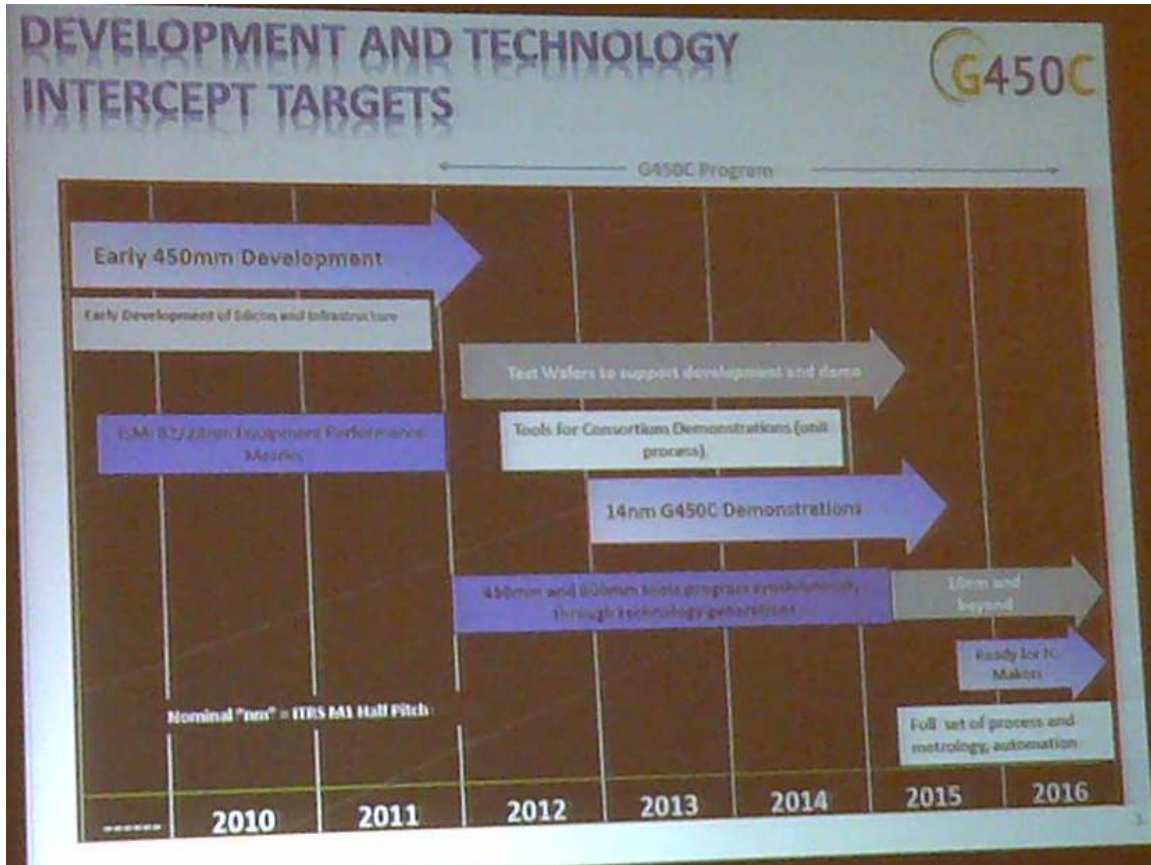
- **SOKUDO DUO Track**
 - Tool on schedule for 4Q2014 Albany, NY delivery
 - Process capabilities include PT develop, NT develop, DSA coating, annealing, UV cure and wet PMMA removal
 - SCREEN is providing 450mm wafer coating and DSA processing service from their Hikone facility
- **Nikon 193i Scanner**
 - First 193i scanner patterned 450mm wafers are being presented at SEMICON West 2014
 - 450mm patterning service being provided to G450C from the Nikon Kumagaya facility
 - Nikon 193i scanner scheduled for delivery to the G450C in Albany, NY in early 2015

SCREEN
SOKUDO DUO X450

Nikon

G450C Schedule

An updated schedule for G450C was also presented at SEMICON West.



A few new publications on metrology and gas flows have appeared on the G450C website at :

<http://www.g450c.org/publications.aspx>

450mm Standards Update

SEMI have published a useful guide to the latest 450mm standards on their website at

<http://www.semi.org/node/50201>

Included are the latest details on the following topics :

- The International Advanced Wafer Geometry Task Force issued ballot 5654 in cycle 2-14, revision to SEMI M49-0613, Guide for Specifying Geometry Measurement Systems for Silicon Wafers for the 130 nm to 16 nm Technology Generations. The purpose is to reduce 450mm wafer edge exclusion from 2 mm to 1.5 mm for 16 nm technology generation. This ballot will be adjudicated at the SEMI North America Silicon Wafer TC Chapter meeting in July 8, 2014 during SEMICON West in San Francisco, California.
- Related to this is doc. 5655 which attempts to increase the Fixed Quality Area (FQA) from 223 mm to 223.5 mm for 450mm polished wafer in SEMI M1-0414 – Specification for Polished Single Crystal Silicon Wafers. These changes are significant since there may be limitations in verifying the quality of wafers close to the wafer edge due to limitations of measurement equipment.
- Doc 5604 on 450mm notchless wafer was mentioned earlier and will be discussed further at SEMICON Europa.
- The Japan Assembly & Packaging Technical Committee (TC) Chapter initiated document 5636 in effort to meet the demand of Automated Material Handling System (AMHS) manufacturers by adding detection area in Tape Frame Release Bar (TFRB) by revising SEMI G92-1113 Specification for Tape Frame Cassette for 450mm Wafer.
- The 450mm International Physical Interface Carriers and International Process Module Physical Interface Joint Task Forces proposed revisions (doc. 5626) to both:
 - SEMI E154-0713 – Mechanical Interface Specification for 450mm Load Port
 - SEMI E166-0513 – Specification for 450mm Cluster Module Interface: Mechanical Interface and Transport Standard

The intent is to improve Equipment Front End Module (EFEM) pocket volume allowing conventional robots to have an extra range of vertical motion.

Other Recent Articles

Despite a slowdown in discussions, the following articles have appeared in the press in recent months. Not all necessarily represent the mainstream view of the 450mm community but are worth a read.

First there are four presentations from SEMICON West on the 450mm Central website. They are in the 'Papers/Presentations/Resources' box on the bottom right of the page.

<http://www.semi.org/en/Issues/450mm>

“450mm Lithography Development Update” - Hamid Zarringhalam, Nikon Precision

(Editorial note : This excellent presentation addresses all the negative points made by some in the industry and is the one to read if you have limited time)

“450 Technology Development and Equipment Performance Metrics” - Paul Farrar and Frank Robertson, G450C

“450mm and Moore's Wall” - G. Dan Hutcheson, VLSI Research

“Industrial Transition to 450mm Notchless Wafers” - Pinyen Lin, G450C

Other articles of interest include :

“450mm transition toward sustainability: Facility and infrastructure requirements” by Adrian Maynes and Frank Robertson of the G450C in Albany, NY,

<http://electroiq.com/blog/2014/06/450mm-transition-toward-sustainability-facility-and-infrastructure-requirements/>

“What Happened To 450mm?” by Mark LaPedus, Ed Sperling & Katherine Derbyshire

<http://semiengineering.com/what-happened-to-450mm/>

“The Macroeconomics of 450mm Wafers” by Apek Mulay

<http://www.semi.org/en/node/50856>

“EUV Is Key To 450mm Wafers” by Katherine Derbyshire

<http://semiengineering.com/euv-is-key-to-450mm-wafers/>

10/100/20

One of the first initiatives under Horizon 2020 is the 10/100/20 initiative announced by Neelie Kroes in 2013. This aims to achieve 20% of world semiconductor production within Europe by 2020.

As a first step the European Leaders Group released their first report on February 2014 and have now released a follow on report entitled “A European Industrial Strategic Roadmap for Micro- and Nano-Electronic Components and Systems - Implementation Plan” detailing their suggestions. This is available to download at :

http://ec.europa.eu/information_society/newsroom/cf/dae/document.cfm?doc_id=6293

Unfortunately no mention is made of 450nm processing and this appears to have been quietly dropped from the goals of this group set by Ms Kroes last year.

Editorial

The views expressed here are those of the editor and not necessarily of other European 450mm project members.

Two years ago the industry was truly excited about 450mm. Some were for it and some were against it but everyone had an opinion and most seemed to be discussing it. Conferences on 450mm were standing room only and articles appeared regularly in the press. This remained the case less than a year ago.

Now however there is no avoiding the fact that 450mm is no longer the hot topic it was. Of course much of this can be put down to the fact that Intel was having delays with its 14nm process, whilst TSMC is in the process of releasing a 20nm planar followed by its 16nm FinFET technology in record time. Meanwhile Samsung appears to be gaining traction with its own 14nm FinFET technology, licensing it to GlobalFoundries when their internal development hit problems, but also licensing 28nm FD-SOI from STMicroelectronics, possibly to avoid the need to actually release a 20nm planar process which the FD-SOI process is expected to outperform both on cost and performance. Indeed at the current time the estimated cost of FD-SOI in full production is probably the biggest discussion point in the industry which is a little unusual for a European developed technology other than lithography.

Understandably with all of this happening most people have no time to discuss 450mm at the present time. But everyone is also now aware that statements made in 2010 by Future Horizons and Broadcom have come true and unlike all previous process nodes, the 20nm and 14nm nodes from foundries will be more expensive per transistor than expected when compared with the costs of 28nm transistors, though they will still have better speed and power characteristics of course.

(As an interesting aside, if you plot the cost per transistor cycles, it is a far straighter line on a log graph than the cost per transistor ever was.)


Mentor Graphics presented the following slide last year.

...Until the 20nm Node?

CHALLENGES TO MOORE'S LAW SCALING

Technology Generation	Normalized Area
45nm	1.0
40nm	~0.6
32nm	~0.45
28nm	~0.3
20nm	~0.2
20 FinFET	~0.2

Technology Generation	Normalized Cost/Transistor
45nm	1.0
40nm	~0.9
32nm	~0.7
28nm	~0.5
20nm	~0.5
20 FinFET	~0.5




Lisa Su,
AMD
ISSCC '13
Keynote

- Lithography challenges begin severely limiting area scaling at 20nm node
 - Fewer 1X metals due to cost
 - Less aggressive feature scaling due to lithography challenges
- Compounded by rapidly increasing lithography costs
 - 28 → 20nm transition is inflection point with dual exposure
 - No cost / transistor crossover for first time at 28 → 20nm transition

© 2013 Mentor Graphics Corp. | February 9th, 2013

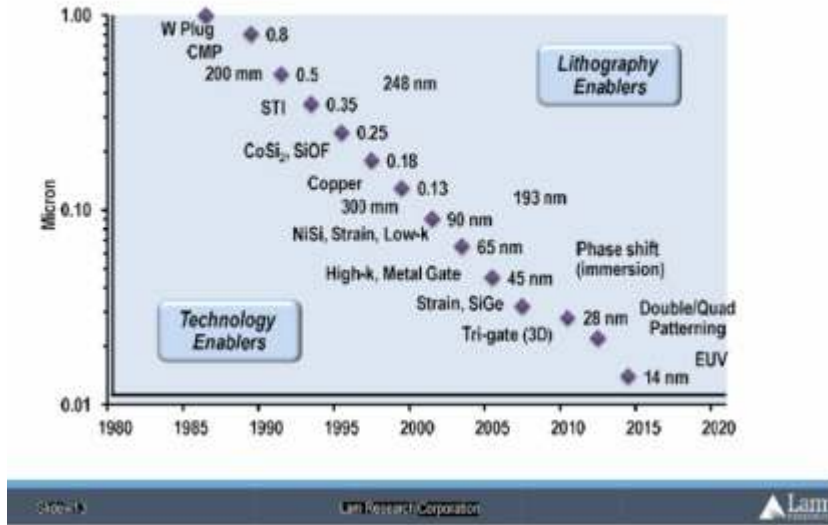
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Our continued following of Moore’s Law has made us used to transistors becoming ever cheaper and this abrupt change has come as a shock to many, with everyone stating that the cost of processing is increasing so rapidly, creating a rash of articles on the “End of Moore’s Law”.

However new processes have always required an extra something and thus have always been more expensive than the previous generations. Some key process improvements over the years are shown in the following figure from Lam and none of these were either easy or inexpensive to implement.

Continuous Innovation Enables Continuation of Moore's Law



Across all the history of our industry these extra costs have gradually built up and threatened the Moore's Law trend and so the industry has always relied on the extra saving of a wafer size increase to bring costs back onto the expected line.

If we look at the following data we can clearly see the contribution made by wafer size.

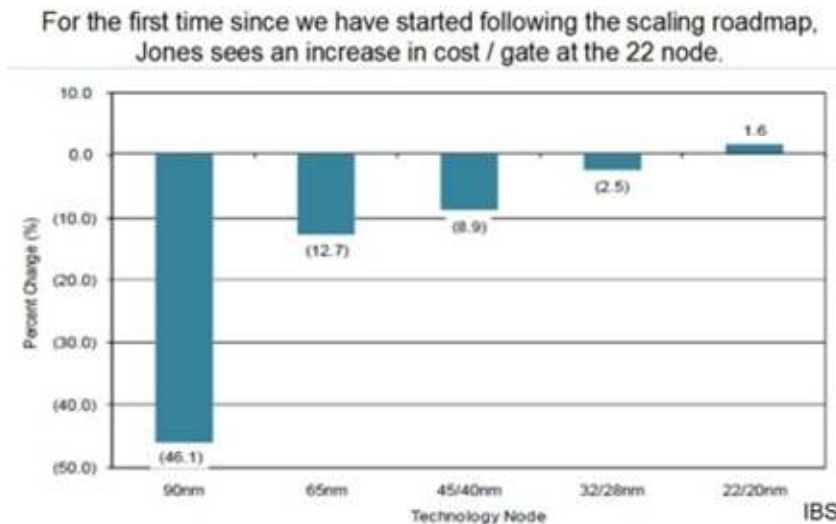
Wafer Size	Commercial Production date
3inch	1975
125mm	1979
200mm	1991
300mm	2001
450mm	2020 ????

There were a few other intervening wafer sizes but as can be seen historically we have achieved a 50 percent increase in wafer diameter roughly every decade. Based on this 450mm should have been introduced in 2011 or 2012 and the expected 20 to 30 percent cost saving would have pushed the 20nm and 14nm processes well back towards the cost curves we have been following for many years.

Alternatively we can ask the converse question, namely what would have happened to the cost of process technologies if we had remained on 200mm wafers ? After all the 300mm transition was no walk in the park with one failed start and the second attempt only succeeding with the considerable support of the German government.

90nm was, and still is, the only technology made on both sizes of wafer and at the time costs were stated by AMD and others as being very similar. But this was early on in the 300mm introduction cycle and so the cost of 300mm wafers and processing equipment was still high. By the time the process was mature, something that took longer than expected due to process issues such as leakage, it can be seen in the following figure below using data from IBS and reproduced by EETimes that the cost saving at this node was way out of line with normal expectations.

Once mature, 300mm was estimated to save around 32 percent compared with 200mm so if we remove 32 percent from the cost of 90nm we can see there is still a cost reduction due to the new process, but it is more in line with that achieved at 65nm.



By the time 65nm was introduced in 2006, 300mm was the only platform used but the unanswered question is how much of the 12.7% cost saving is due to the reduced process sizing and how much is due to continued optimisation and cost reduction of the 300mm platform ? We accept neither of these nodes would have actually achieved a price per transistor increase without 300mm but the lower price decrease would have put Moore’s Law in doubt a decade earlier.

Around this same time, it was already being realised that the 300mm platform was certainly not optimal in cost terms and discussions on a “300mm Prime” initiative began. In parallel with this, the length of time it had taken to achieve the 300mm transition made the industry realise it had to begin discussing the next transition as well. This soon settled on a 450mm size but everything else was up for debate.

Unfortunately the costs of either greatly concerned the semiconductor equipment industry who had yet to achieve a payback from the two attempts standard 300mm equipment took to develop, whilst the rest of the industry broke into two camps with neither making much progress. Of course neither 300mm processing equipment development nor fab design has not stood still and performance enhancements and cost savings have been achieved, but the fact remains that to remain on the cost curves attributed to Moore’s Law a wafer transition is now overdue.

We believe the transistor pricing issue could have been foreseen far earlier, but in fact it was 2011 or 2012 before it was being openly discussed, and then still often met with deep scepticism. By this time the industry had divided into pro- and anti- 450mm camps and there has been little movement in opinion since then. This hasn’t been helped by Intel recently claiming they are still on the historic pricing curve but their cost models are rather different to those of the foundries who serve most of the industry.

We thus assert that without a transition to 450mm then the costs per transistor could rise again at some future nodes and although cost reductions will still be achieved, the graphs will continue to show erratic rather than a smooth transition downwards.

Memories

A statement that we now see being made repeatedly is that “memory devices are going 3D and don’t need 450mm”. This follows on from the assumption that a new wafer size is only used at the leading edge node and the move to 3D has made device geometries much larger. However Infineon has shown that 300mm wafers are advantageous even for power device geometries.

Our costing models suggest were it available now, 450mm would be equally advantageous for the new 3D Flash devices. Indeed at earlier wafer transitions, memory has often been the lead product and we can conceive of no situation other than a lack of equipment whereby memory devices will not eventually make the transition to 450mm. Indeed were one memory manufacturer to make the jump, the others would have to follow quickly or be locked out of the market as there are no more cost sensitive markets than DRAM and Flash.

EUV & Other Equipment

Ever since we were first involved in 450mm discussions, we have been concerned that the 450mm wafer size has become entwined with EUV lithography. Of course we all accept it would be convenient if both were introduced to full production at the same time but not every layer needs EUV processing and 450mm immersion and possibly non-immersion litho machines will still be required. Nikon are delivering the first prototype of such a device soon and we expect this will be made production ready as soon as orders are placed.

Other equipment is also moving through R&D towards production readiness and it only needs one semiconductor manufacturer to hit the 'go' button and place orders and the 450mm equipment industry will spring into life.

In the meantime what we are seeing is that equipment where 450mm wafers can be accommodated at little extra cost is beginning to appear, an example being the KLA-Tencor SP3 Unpatterned Wafer Surface Inspection Systems.

Current Status

Of course no semiconductor company is going to build a 450mm fab unless they have the products to fill it. And one downside of 450mm is that you are building fab modules with significantly more capacity than 300mm ones. Another problem is that wafers of a new larger size always cost more per unit area early on and combined with the extra effort needed to introduce larger wafer processing, few companies have the resources to take the pain whilst waiting for the gain.

Intel

At the current time Intel is about to shrink many of their products down to the new 14nm process but still sell than at around the same price. Even allowing for the extra demands of double patterning, this will mean they need less fab capacity to keep their current sales and the released capacity can be used for other markets as they have seeking to do in recent years. Once this capacity is filled they have Fab 42 in Arizona ready to be equipped which would take about a year to generate more capacity, whilst the Israel fab will be in line for an upgrade as well.

Intel state they are still committed to 450mm so it really depends on how quickly the company's foundry sales progress as to when a decision needs to be made on which wafer size is installed. But without 450mm processing we suspect their cost structures may be too high to be able to win large volume foundries orders from the likes of Apple

so they are in a chicken and egg situation. We thus expect Intel will be looking for extra support than is usual from government organisations to make the transition.

Conversely we would be surprised if long time Intel supplier Nikon would be making such large and public investments in 450mm litho unless it had a strong expectation that Intel would place orders with it.

In the meantime we believe construction is continuing on its D1X module 2 which will prototype 450mm technology but there are several processing jobs advertised for a D1X module 3.

Samsung

Samsung has never been vocal on 450mm but obviously needs to keep track of what the other two major companies are doing. It already has a major share of the memory market due to its lower cost structures so is under less pressure to change wafer size. But it has lost long time customer Apple for the current generation A8 processor though rumour is it has won at least part of the following contract for the A9. We suspect this is a little early and Apple will currently be comparing FinFET processes from Intel, Samsung and TSMC before making a decision. Time will tell on this but unless Samsung does win this contract it probably has too much logic capacity available.

DRAM wafer area usage is remaining fairly static and there is oversupply in the market driving down prices, mainly due to Samsung switching the Line-17 logic fab to DRAM production.

However in NAND Flash the move to SSDs (solid state drives) is now in full swing and demand is expected to grow considerably. The company has two competing approaches to address this market, standard MLC Flash shrunk to 1x nm dimensions and 3D stacked SLC Flash using 32 layers of 3x class devices. The first approach needs the most advanced lithography whilst the second uses far larger amounts of older lithography techniques. In the longer term we expect 3D Flash to become the most cost effective solution and the timescales for this happening could coincide with 450mm equipment becoming production ready. Once the costs of the transition are absorbed, the lower production costs of 450mm would give them a trump card over competing 3D Flash from Hynix, Micron and Toshiba/SanDisk.

TSMC

TSMC is the company currently most overloaded. The winning of the Apple A8 contract means it has had to produce around a quarter of a million extra wafers in short time whilst still trying to satisfy its existing customers. Industry rumours state that they

haven't achieved this too well and some major customers are now looking elsewhere for capacity. TSMC has announced new capex to try to raise capacity in existing facilities but this is the company that most looks like it needs a new fab at the current time.

But 450mm equipment will not be production ready in the timescales we expect TSMC to need to address its current shortfall and so the introduction of 450mm by TSMC depends on them carrying on winning very large volume orders, but the location of such a fab is now approved as mentioned earlier.

Finally rumours that TSMC would build a fab in New York State appear to have died away, at least for now.

Others

3D Flash is the one area where we can see that with the appropriate support Hynix or Toshiba could make the transition to 450mm. But of course both look at Infineon/Immondo's plight after the first introduction of 300mm processing and wonder if they have the resources to avoid the same fate and we would tend to agree with them on this.

Apart from TSMC, logic foundries are nowhere near profitable enough at the present time to even consider making the jump to 450mm.

Conclusions

There are many in the industry quite loudly stating that 450mm isn't justified until at least 2025 to 2030 timeframe, if at all. But of course the same thing was said back in the mid-1990s about 300mm and I think all will accept that has been a good thing for the industry.

Future Horizons suggests this is too pessimistic and simply reflects the current near-term business, financial and technical issues the industry is facing. Once these issues are dealt with we believe one of the big three will decide to seize the 450mm competitive advantage and it will be back on the agenda with a vengeance.

However we can be sure this company will be looking for significant government support to help bear the pain of making the transition first. To assist with this one possibility we have considered is that one of the companies will make an agreement with the key equipment suppliers for up to two years so as to allow them to amortise the cost of the transition before others benefit from their expenditure thereby avoiding a repeat of what happened at 300mm.

Of course what everyone would like to know is when the transition to production will take place so that plans can be laid. Unfortunately it depends on so many parameters but we believe it will be far closer to 2018 than 2025. Only time will tell if we are correct.